DATA SHEET

Power Your Critical Mission Today

# SVPL1209S SERIES

## SPACE QUALIFIED POINT OF LOAD CONVERTERS


SVPL1209S – Exact marking may differ from that shown

**Models Available**

| |
|---|
| Input: 3.1 V to 13.2 V |
| Output Range: 0.8 to 5.0 V, 9 A |
| Qualified to MIL-PRF-38534 Class H and Class K; RHA level R |

## 1.0 DESCRIPTION

The SVPL Series of space qualified point-of-load DC-DC converters is specifically designed for the harsh radiation environment of space applications. Performance is guaranteed through the use of hardened semiconductor components and analysis. The SVPL Series has been characterized for Total Ionizing Dose (TID) performance including Enhanced Low Dose Rate Sensitivity (ELDRS) and for Single Event Effects (SEE) per VPT's DLA-approved Radiation Hardness Assurance (RHA) plan per MIL-PRF-38534, Appendix G, Level R.

The SVPL1209S is based on the Intersil ISL70003ASEH radiation-hardened monolithic buck regulator. It is designed to operate from nominal bus voltages from 3.3 V to 12 V. The SVPL1209S supplies low voltages at 9 A with high efficiency and fast transient response, making it an ideal choice to supply point-of-load applications such as high performance space processors.

## 1.1 FEATURES

- Operates from 3.1 – 13.2 V input
- Adjustable Output from 0.8 – 5 V
- Up to 9 Amps Output
- High Efficiency, up to 93%
- High Power Density, up to 144 W/in$^3$
- Output Enable Control
- Low Output Noise
- Over Current Protection
- Synchronizable to an external clock

## 1.2 SPACE LEVEL CHARACTERIZATIONS

- Total Ionizing Dose Performance
  - High Dose Rate [50-300 rad(Si)/s] ≥ 100 krad(Si)
  - Low Dose Rate [<10 mrad(Si)/s] ≥ 100 krad(Si)
- Single Event Effects Performance
  - SEL, SEB, and SEGR $LET_{TH}$ ≥ 85 MeV/mg/cm$^2$
  - SEFI Threshold $LET_{TH}$ ≥ 42 MeV/mg/cm$^2$
  - SEFI X-section ($LET_{EFF}$ = 85 MeV/mg/cm$^2$) ≤ 1.18x10$^{-7}$ cm$^2$
  - SET fully characterized for cross section and magnitude
- Operation from -55 °C to +125 °C
- Worst-case analysis, stress, radiation, reliability reports available

## 1.3 MANUFACTURING AND COMPLIANCE

- Qualified to MIL-PRF-38534 Class H and Class K, DLA SMD # 5962-17231
- MIL-PRF-38534 element evaluated components
- Manufactured in a MIL-PRF-38534 Class H and Class K facility
- MIL-STD-883
- ISO-9001

## 1.4 PACKAGING

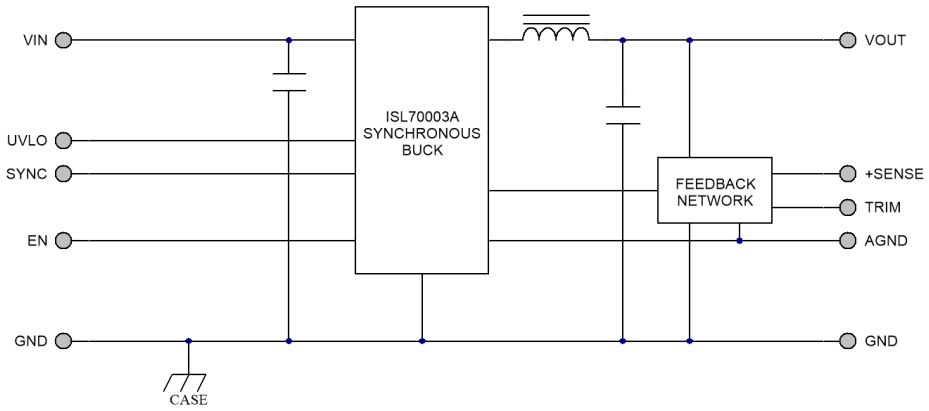
- Low-profile: 1.075" x 1.075" x 0.270"
- Max weight: 18 g
- Precision projection-welded hermetic metal case

## 1.5 SIMILAR PRODUCTS AND ACCESSORIES

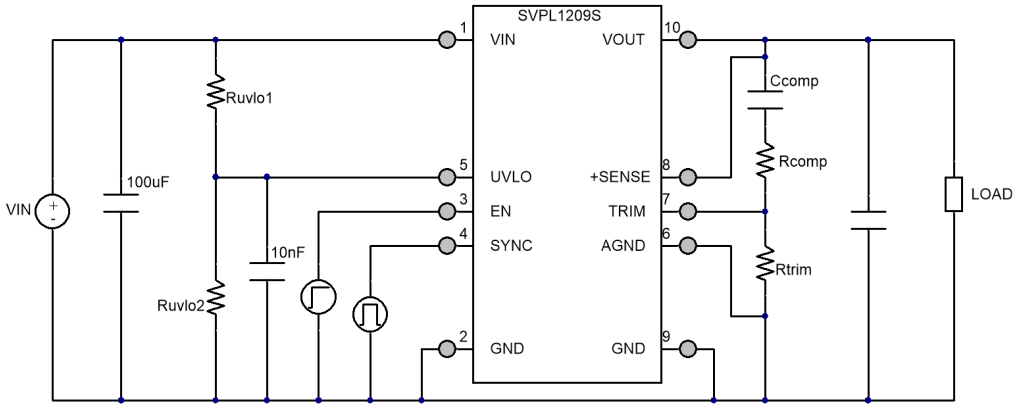
- SVPL3R306S 6 A space qualified point of load DC-DC converter
- SVPL3R312S 12 A space qualified point of load DC-DC converter
- SVGA0510S 10 A space qualified point of load DC-DC converter
- SVGA0515S 15 A space qualified point of load DC-DC converter
- Custom versions available
- Space qualified isolated DC-DC converters, 6 - 100 W

## 2.0 DIAGRAMS

### 2.1 BLOCK DIAGRAM




### 2.2 CONNECTION DIAGRAMS




1. Rtrim should be connected directly across pins 6 and 7 as close as possible to the SVPL.
2. AGND should be connected to GND close to the SVPL. Voltage difference between the AGND and the GND pins greater than 0.3 V may result in regulation error and/or damage to the SVPL.
3. If not using EN and VIN ≤ 5.15 V, pin 3 can be connected directly to VIN. For VIN > 5.15 V, pin 3 can be pulled up toward VIN through a 49.9 kΩ - 100 kΩ resistor.
4. If not synchronizing converters, connect pin 4 to GND.
5. Rcomp and Ccomp are optional components that can be used to optimize the SVPL transient response.

## 3.0 SPECIFICATIONS

### 3.1 ABSOLUTE MAXIMUM RATINGS

| Absolute Maximum Ratings | | | |
|---|---|---|---|
| VIN[1]: | -0.3 V to 16 V | Operating Temperature (Full Load): | -55 °C to +125 °C |
| EN, UVLO, SYNC[2]: | -0.3 V to 5.15 V or to VIN + 0.3 V | Storage Temperature: | -65 °C to +150 °C |
| AGND: | -0.3 V to 0.3 V | Lead Solder Temperature (10 seconds): | 270 °C |
| ESD Rating per MIL-PRF-38534: | 1B | | |

1. VIN limited to 13.7 V for operation in a heavy ion environment at LET ≥ 85 MeV/mg/cm$^2$ and Tcase = 125 °C. Derate VIN ≤ 12.5 V to comply with MIL-HDBK-1547.
2. EN, UVLO, and SYNC must be limited to 5.15 V or to VIN + 0.3 V, whichever is lower. EN can be pulled up toward voltages higher than 5.15 V through a 49.9 kΩ - 100 kΩ resistor.

## 3.2 PERFORMANCE SPECIFICATIONS[1]

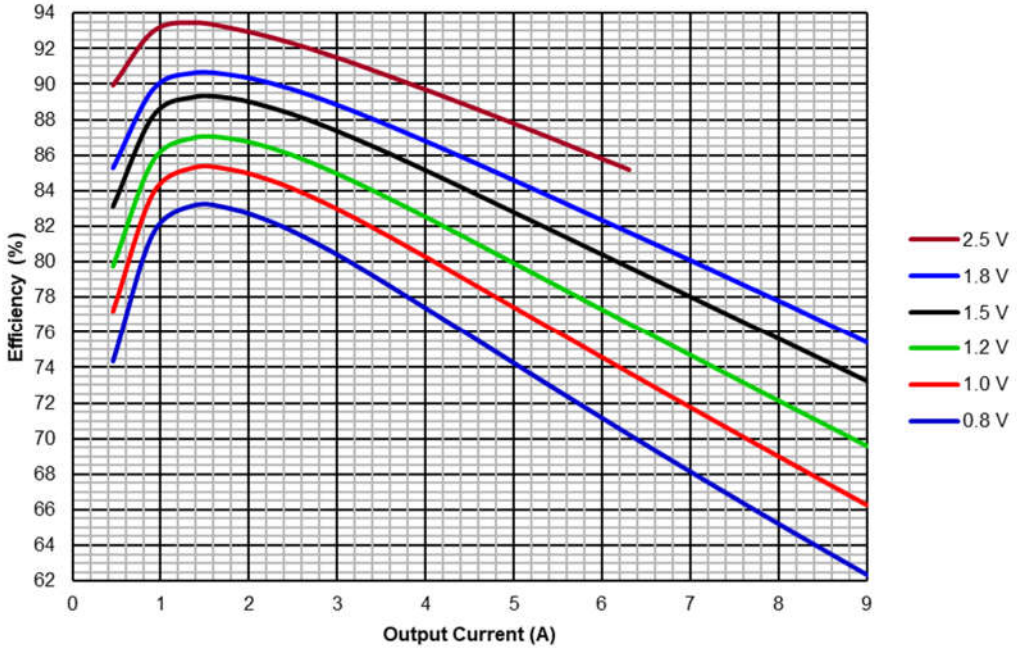
Tcase = -55 °C to +125 °C, Vin = 3.3 V ± 1% or 5 V ± 1% or 12 V ± 1%, Full Load, Unless Otherwise Specified

| | | SVPL1209S | | | |
|---|---|---|---|---|---|
| **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Units** |
| **INPUT** | | | | | |
| Voltage[2] | | 3.1 | - | 13.2 | V |
| Current | EN = GND, Vin = 3.3 V | - | 1.3 | 7 | mA |
| | EN = GND, Vin = 5 V | - | 2 | 7 | mA |
| | EN = GND, Vin = 12 V | - | 4 | 7 | mA |
| | Vin = 3.3 V, No Load | - | 40 | 60 | mA |
| | Vin = 5 V, No Load | - | 50 | 75 | mA |
| | Vin = 12 V, No Load | - | 90 | 125 | mA |
| Undervoltage Lockout[2] | UVLO Reference Voltage | 0.55 | 0.6 | 0.65 | V |
| | UVLO Sink Current | 8.9 | 12 | 15.1 | µA |
| **OUTPUT STATIC** | | | | | |
| Voltage | Tcase = 25 °C | -1.0 | - | +1.0 | %Vout |
| | Tcase = -55 °C to +125 °C | -1.5 | - | +1.5 | %Vout |
| Power[3] | | 0 | - | 45 | W |
| Current[4] | Tcase = -55 °C to +95 °C | 0 | - | 9 | A |
| | Tcase = +125 °C | 0 | - | 6 | |
| Ripple Voltage | Vin = 3.3 V, Vout = 1.8 V, 20 Hz to 10 MHz | - | 30 | 60 | mVpp |
| | Vin = 5 V, Vout = 3.3 V, 20 Hz to 10 MHz | - | 35 | 60 | mVpp |
| | Vin = 12 V, Vout = 5 V, 20 Hz to 10 MHz | - | 85 | 120 | mVpp |
| Load Regulation | | -0.6 | 0.03 | +0.6 | %Vout |
| Load Fault Dissipation | Vin = 12 V, Vout = 5 V | - | - | 6 | W |
| **OUTPUT DYNAMIC** | | | | | |
| Load Step, Half to Full Load, Vin = 5 V, Vout = 3.3 V | Output Transient | - | 75 | 140 | mV |
| | Recovery[5] | - | 150 | 300 | µs |
| Turn-On (Vin = 0 to 3.3 V or 5 V or 12 V, EN = Vin) | Delay | - | 6 | 10 | ms |
| | Overshoot | - | 0 | 15 | mVpk |
| **FUNCTION** | | | | | |
| Enable (EN)[2] | EN Input High Voltage | 2.1 | - | - | V |
| | EN Input Low Voltage | - | - | 0.7 | V |
| SYNC Frequency Range[2] | | 420 | - | 580 | kHz |
| **GENERAL** | | | | | |
| Efficiency | Vin = 5 V, Vout = 3.3 V | 81 | 87 | - | % |
| Capacitive Load[2] | Vout ≤ 1.2 V | - | - | 5000 | µF |
| | Vout ≥ 1.2 V | - | - | $\frac{6000}{Vout}$ | |
| Switching Frequency | | 425 | 500 | 575 | kHz |
| Weight | Standard package option | - | - | 18 | g |
| MTBF (MIL-HDBK-217F) | SF @ Tcase = 55 °C | - | 5.77 | - | MHr |
| **POST-RAD END-OF-LIFE LIMITS[6]** | | | | | |
| OUTPUT Voltage | Tcase = -55 °C to +125 °C | -3.0 | - | +3.0 | %Vout |
| Switching Frequency | | 420 | - | 580 | kHz |

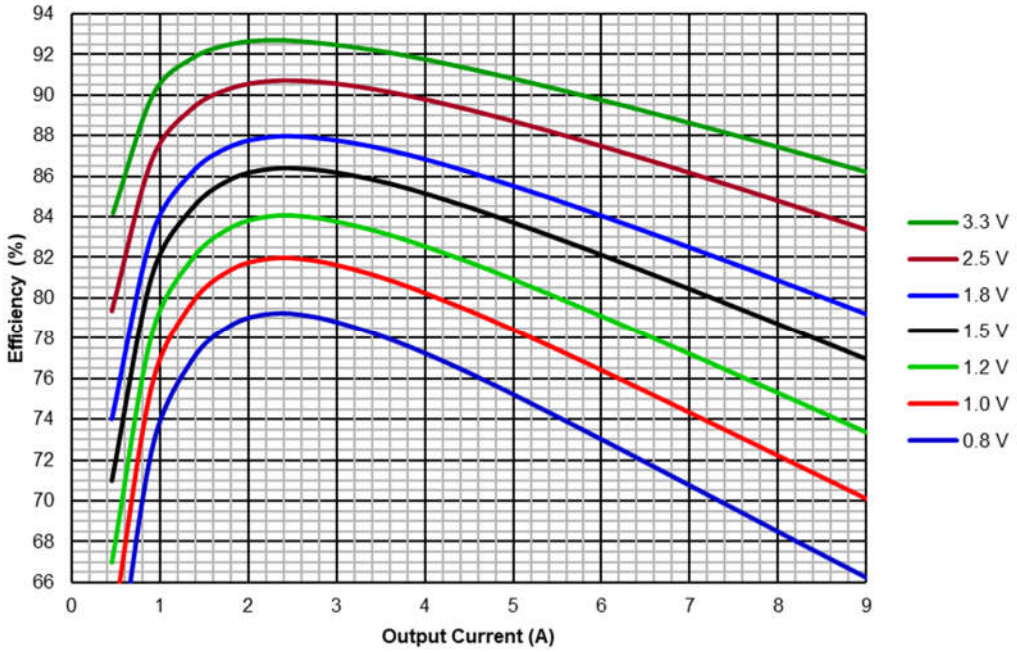
1. Performance specifications are guaranteed with 100 µF from VIN to GND.
2. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.
3. Dependent on output voltage.
4. Output current is rated to 9 A for Tcase ≤ 95 °C. From 95 °C to 125 °C, derate linearly from 9 A to 6 A.
5. Time for output voltage to settle within 1% of steady-state value.
6. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted.

## 4.0 PERFORMANCE CURVES

### 4.1.1 SVPL1209S Efficiency (Typical, 25 °C, Vin = 3.3 V)

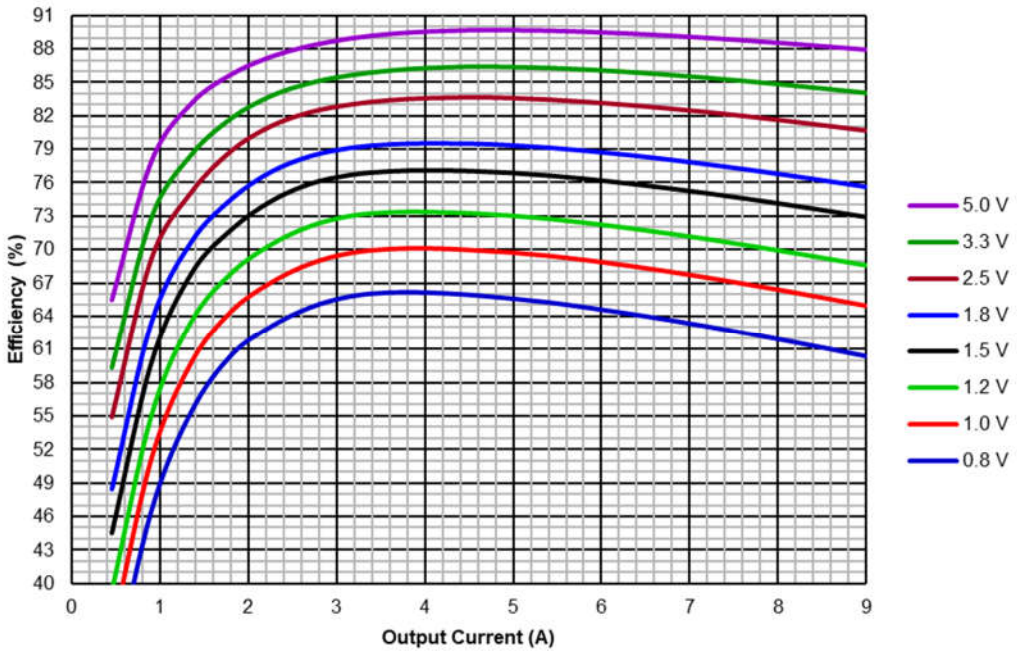



### 4.1.2 SVPL1209S Efficiency (Typical, 25 °C, Vin = 5 V)



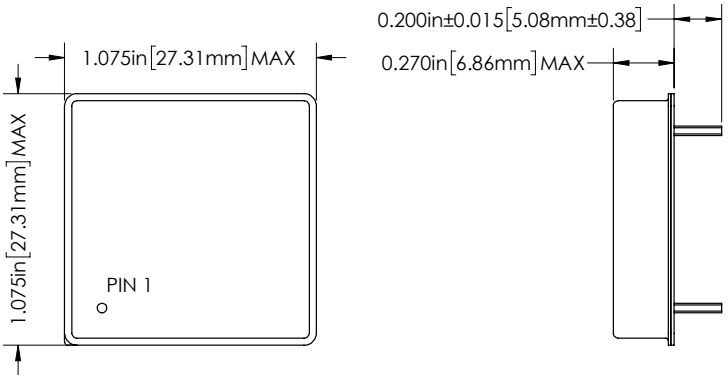
## 4.0 PERFORMANCE CURVES (CONTINUED)

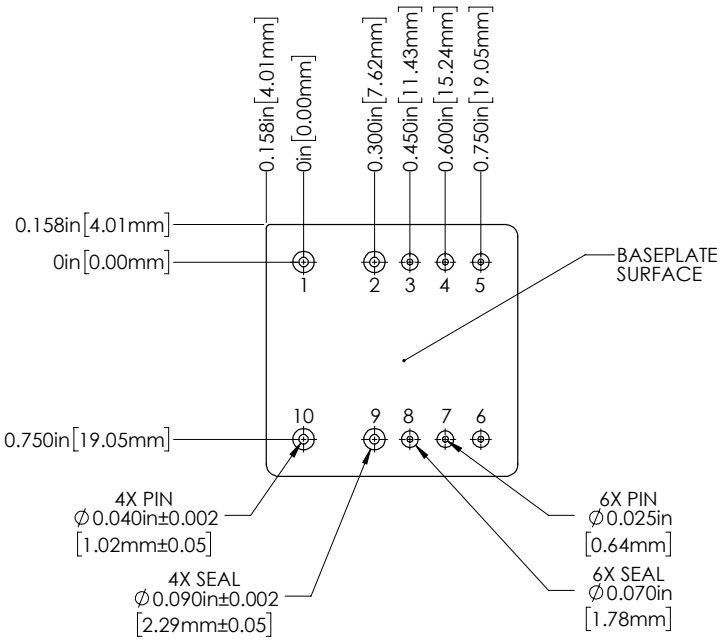
### 4.2.1 SVPL1209S Efficiency (Typical, 25 °C, Vin = 12 V)



## 5.0 MECHANICAL OUTLINES AND PINOUT

**Standard Package:**




1. Tolerances are ±0.005" unless otherwise stated.
2. Case temperature is measured on the center of the baseplate surface.
3. Materials: Case (Steel, gold over nickel plated); Cover (Steel, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated); Pin Seals (Glass).

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | VIN | 6 | AGND |
| 2 | GND | 7 | TRIM |
| 3 | EN | 8 | +SENSE |
| 4 | SYNC | 9 | GND |
| 5 | UVLO | 10 | VOUT |

## 6.0 TECHNICAL NOTES


Please note that many of these functions are also demonstrated in detail on the VPT website in the form of technical video labs.

## 6.1 GENERAL INFORMATION

### 6.1.1 Topology Description

The SVPL1209S is a non-isolated, fixed-frequency, radiation-hardened, synchronous buck converter based on the Intersil ISL70003ASEH. It is optimized for low voltage point-of-load (POL) applications. The SVPL1209S operates from a 3.1 to 13.2 V input and provides a stepped-down, precisely regulated, programmable output voltage at high efficiency.

### 6.1.2 Source Impedance

The impedance of the input source can interact with the POL converter and impact performance. High source impedance is often caused by a long input cable or other components added in series with the input. In some cases, additional input capacitance will be needed to stabilize the system.

### 6.1.3 Case Connection

The SVPL1209S case is connected to GND at a single point inside of the package.

## 6.2 FUNCTION DESCRIPTIONS

### 6.2.1 Enable (EN)

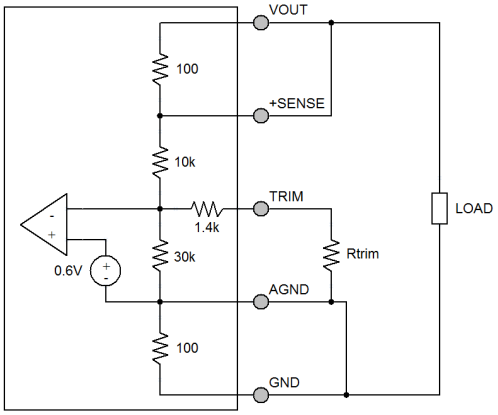
The EN pin accepts TTL/CMOS logic input as described in the Performance Specifications table. When EN is pulled low, the converter is disabled and the supply current drops to typical values between 1.3 – 4 mA, depending on the input voltage. The internal power MOSFETs will be turned off, and the SVPL1209S power stage will be in a high-impedance state. When the EN pin voltage exceeds its logic rising threshold, the SVPL1209S monitors the UVLO pin voltage before initiating soft-start. The EN pin should not be driven higher than 5.15 V. If the EN signaling voltage is higher than 5.15 V, use a 49.9 kΩ – 100 kΩ resistor in series with the EN pin. If ON/OFF capability is not required and Vin ≤ 5.15 V, EN can be connected directly to Vin. If Vin > 5.15 V, EN can be pulled up toward Vin through a 49.9 kΩ – 100 kΩ current limiting resistor.

### 6.2.2 Synchronization (SYNC)

The SVPL1209S can be synchronized to an external clock with a frequency range of 500 kHz ±15%. During start-up, the converter will use its internal oscillator. Once soft-start is complete, the converter will synchronize to the external clock signal. This allows the SVPL1209S to be the power source to the external clock components without the requirement that a clock signal be present at the SYNC pin before start-up. The clock signal's low level must be less than 0.7 V and its high level must be between 2.1 V and 5.15 V to guarantee proper synchronization. The clock signal's duty cycle should be between 40 to 60%. If not synchronizing converters, connect SYNC to GND.

### 6.2.3 Adjusting the Output Voltage (TRIM)

The output voltage of the converter is set with an external trim resistor connected from the TRIM pin to the AGND pin. Use the equations or table below to choose the trim resistor value. Trim resistor tolerance of 0.1% is recommended to achieve an accurate output voltage. The default output voltage with the TRIM pin left open is 0.8 V.




$$R_{TRIM} = \frac{6000}{V_{OUT} - 0.8} - 1400$$

$$V_{OUT} = \frac{6000}{R_{TRIM} + 1400} + 0.8$$

| SVPL1209S | |
|---|---|
| **+Vout (V)** | **Rtrim (Ω)** |
| 0.8 | Open |
| 0.9 | 58.6k |
| 1.0 | 28.6k |
| 1.2 | 13.6k |
| 1.5 | 7.17k |
| 1.8 | 4.60k |
| 2.0 | 3.60k |
| 2.5 | 2.13k |
| 2.8 | 1.60k |
| 3.0 | 1.33k |
| 3.3 | 1.00k |
| 4.0 | 475 |
| 5.0 | 28.6 |

### 6.2.4 Output Capacitors

Output capacitors for point-of-load (POL) DC/DC converters should be chosen to meet output voltage ripple and transient requirements. Meeting the transient response requirement is accomplished by making the output impedance of the converter sufficiently small. Given the high control bandwidth of POL converters like the SVPL series, the peak output impedance is typically dominated by the equivalent series resistance (ESR) of the bulk output capacitance. Therefore, the output capacitors should be chosen to set a certain maximum total ESR. The total ESR is the parallel combination of the internal bulk capacitor's ESR and that of the added capacitors. Given the output voltage transient requirement, maximum load step, and the ESR of each bulk capacitor that will be added, the number of added capacitors needed is calculated with the following equations:

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}}$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}}$$

| Parameter | Definition |
|---|---|
| $\Delta V_{OUT}$ | Max $V_{OUT}$ transient allowed |
| $\Delta I_{OUT}$ | Max load current step |
| $ESR_{TOTAL}$ | Total combined parallel ESR, including internal and added capacitors |
| $ESR_{ADDED}$ | Combined parallel ESR of the added capacitors |
| $ESR_{INTERNAL}$ | ESR of the internal bulk capacitor (**43.7mΩ max** under worst-case conditions) |
| $ESR_{EACH}$ | ESR of each of the added capacitors |
| N | Number of added capacitors |

Make sure that the added capacitance does not violate the maximum allowed output capacitance using the following equation:

$$C_{OUT-MAX} = \frac{6000\mu F}{V_{OUT}}$$

For example, assume that $V_{OUT}$ is 1.5 V, the maximum output transient allowed is 37.5mV, and the load step is 4.5 A. Assume the output capacitors being used are 330 µF and have a maximum ESR of 50 mΩ each.

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{37.5mV}{4.5A} = 8.33m\Omega$$

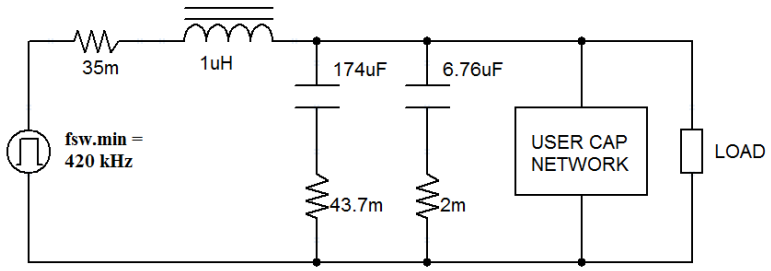
$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}} = \frac{8.33m\Omega * 43.7m\Omega}{43.7m\Omega - 8.33m\Omega} = 10.30m\Omega$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}} = \frac{50m\Omega}{10.30m\Omega} = 4.85 \rightarrow use\ 5\ output\ capacitors$$

$$C_{OUT-MAX} = \frac{6000\mu F}{V_{OUT}} = \frac{6000\mu F}{1.5} = 4000\mu F$$

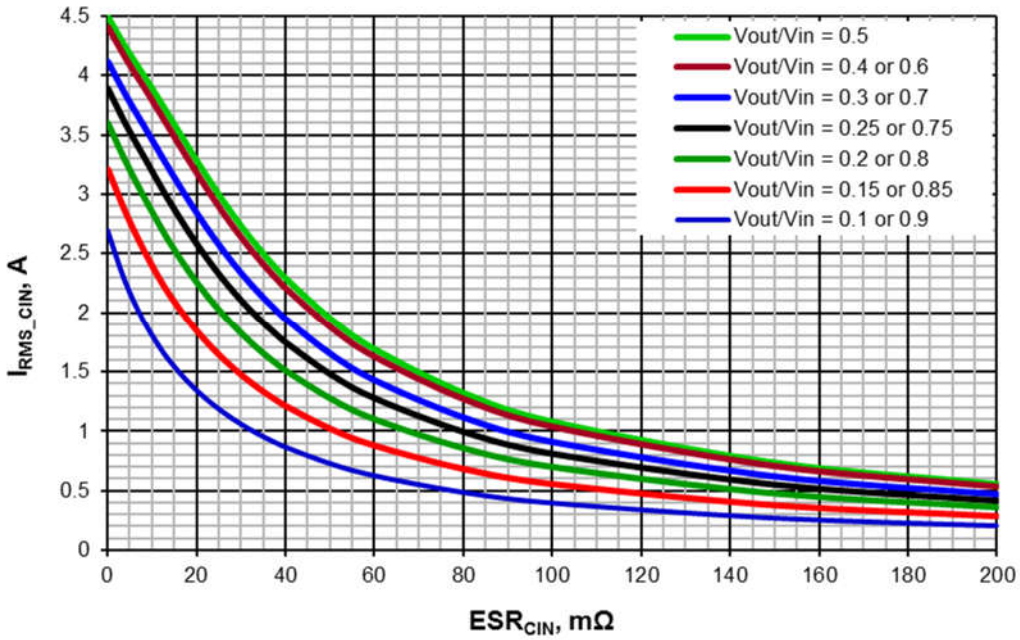
In the example, 5x 330 µF/50 mΩ capacitors are needed. This is a total capacitance of 1650 µF, which is well below the 4000 µF maximum allowed.

The output voltage ripple can be evaluated through simulation using the circuit below. This circuit incorporates worst-case conditions that include the effects of component tolerances, temperature extremes (-55 °C to 125 °C), radiation (100 krad), and aging (10 year mission). Note that the resistor shown in series with the inductor includes the resistance of the inductor and ISL70003A power FETs. The pulsed voltage source should have a peak voltage equal to the input voltage and the minimum switching frequency (420 kHz) to evaluate the worst-case ripple. The duty cycle should be adjusted to attain the correct output voltage.




**6.2.5 Input Capacitors**

A minimum input capacitance of 100 µF should be added between VIN and GND to maintain the input voltage during transient conditions. The SVPL1209S has been designed with internal ceramic input capacitors to minimize the voltage stresses on its power MOSFETs. These ceramic capacitors also reduce the current stress in the user-added input capacitors. For 100 µF or greater capacitors, the RMS currents of the added capacitors will be determined primarily by their combined ESR. The curves below estimate the total RMS current in the added input capacitors for different $V_{OUT}/V_{IN}$ ratios. Worst-case conditions for load current, internal capacitance, and switching frequency are used. To verify the capacitors will have sufficient margin, the RMS current ratings of the added capacitors can be compared to the appropriate curve. If the application $V_{OUT}/V_{IN}$ ratio is between two curves, use the curve with higher RMS current to be conservative. If multiple capacitors are added, then the RMS current will divide between them. If the maximum application load current is less than the SVPL1209S maximum of 9 A, then the RMS current will be reduced proportionally.




For example, let us assume Vin = 5 V, Vout = 1.8 V, max Iout = 5 A, and maximum temperature = 85 °C. Also, assume the capacitor being considered is a 150 µF capacitor with an ESR of 30 mΩ at 85 °C and the worst-case minimum switching frequency of 420 kHz. Assume the capacitor's RMS current rating is 2.7 A at 85 °C. First, determine the Vout/Vin ratio:

$$\frac{V_{out}}{V_{in}} = \frac{1.8V}{5V} = 0.36$$

The ratio lies between the 0.3 and 0.4 curves. Use the Vout/Vin = 0.4 curve, as it has higher RMS current and gives a more conservative estimate. At 30 mΩ, the 0.4 curve indicates an RMS current of 2.65 A. The RMS current for this application is found as:

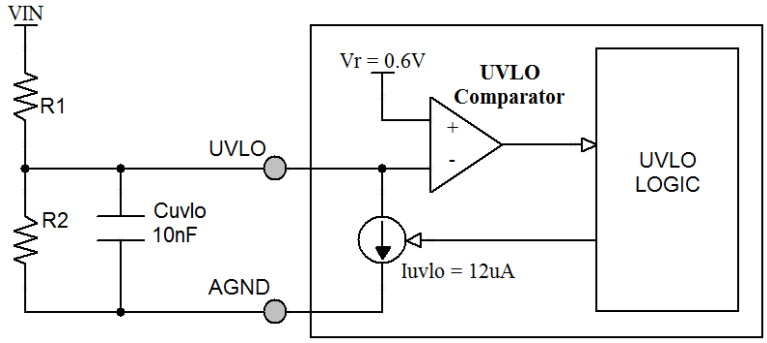
$$I_{RMS\_CIN} = I_{RMS\_CURVE}\left(\frac{Application\ \max I_{out}}{SVPL\ \max I_{out}}\right) = 2.65\left(\frac{5A}{9A}\right) = 1.47A$$

The RMS current in the added input capacitors is 1.47 A, which is 54% of the 2.7 A current rating. The power dissipated in the capacitor will be about 30% of its power rating ($0.54^2 = 0.30$).

## 6.3 PROTECTION FEATURES

### 6.3.1 Input Undervoltage Lockout

The SVPL1209S Series provides input undervoltage lockout (UVLO) protection. For input voltages below the turn-on voltage, the converter will remain off. The internal power MOSFETs will be turned off, and the SVPL1209S power stage will be in a high-impedance state. When the input voltage exceeds the turn-on voltage, the converter will soft-start. For input voltages above the UVLO turn-off voltage but below the operating range of the converter, the converter may reach its maximum duty cycle and the output may be out of regulation. The figure below demonstrates the UVLO circuit. Note that it is referenced to AGND.




Initially, the input voltage (VIN) is below the turn-on threshold ($V_{UVLO\_ON}$) and the $I_{UVLO}$ current sink is active. $I_{UVLO}$ is only active when the voltage at the UVLO pin is less than the UVLO reference voltage, $V_R$. As VIN rises, the UVLO turn-on threshold is calculated as:

$$V_{UVLO\_ON} = V_R \cdot \left[1 + \frac{R_1}{R_2}\right] + I_{UVLO} \cdot R_1$$

After VIN reaches $V_{UVLO\_ON}$, $I_{UVLO}$ turns off. With the part enabled and $I_{UVLO}$ off, the converter will shut down if VIN falls below the UVLO turn-off threshold ($V_{UVLO\_OFF}$):

$$V_{UVLO\_OFF} = V_R \cdot \left[1 + \frac{R_1}{R_2}\right]$$

The undervoltage lockout circuit hysteresis is:

$$V_{UVLO\_HYS} = V_{UVLO\_ON} - V_{UVLO\_OFF} = I_{UVLO} \cdot R_1$$

$R_1$ and $R_2$ are chosen to set the desired thresholds and hysteresis. Typical and extreme values of $V_R$ and $I_{UVLO}$ are provided in section 3.2. The UVLO pin should be bypassed to AGND with a 10nF capacitor to mitigate SEE.

### 6.3.2 Output Soft-Start

The SVPL1209S Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately 4 ms. The soft-start function is active whether the module is turned on with an application of input voltage or from driving EN high. The turn-on delay time is specified from the application of input voltage (or application of EN) until the output reaches 90% of its final value.

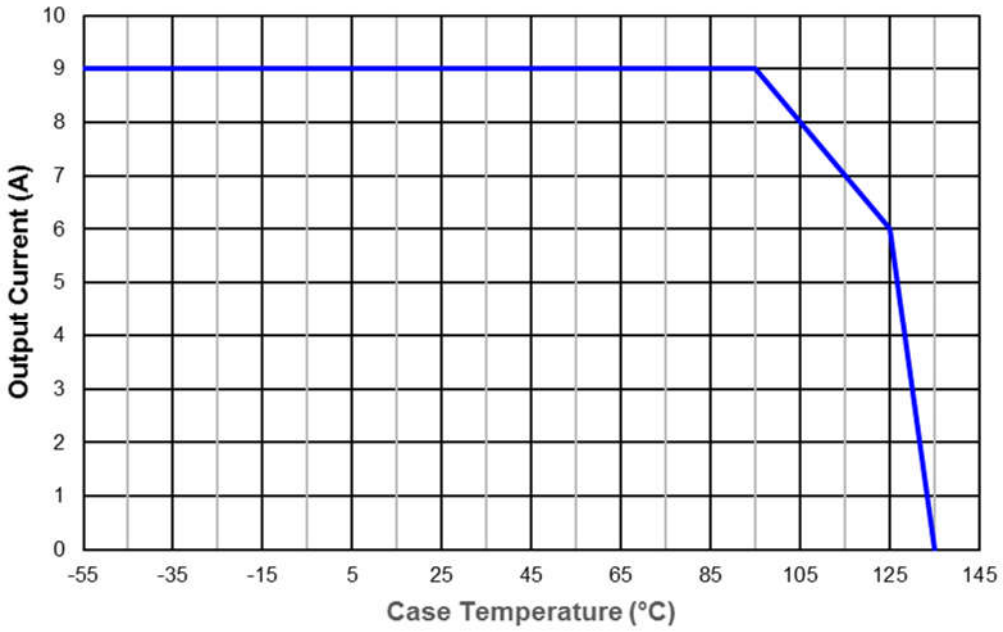
### 6.3.3 Output Short Circuit Protection

The SVPL1209S Series provides hiccup-mode output short-circuit protection. When a sustained high peak current is detected, the converter will shut down. After a delay, the converter will attempt a soft-start. This sequence will continue until the fault is removed, allowing the converter to soft-start and resume normal operation.

## 6.4 THERMAL CONSIDERATIONS

The SVPL1209S output current rating versus case temperature is illustrated in the figure below. It is rated at 9 A for case temperatures up to 95 °C. From 95 °C to 125 °C, derate linearly from 9 A to 6 A. From 125 °C to 135 °C, derate linearly to 0 A. The case temperature of the converter is specified on the baseplate of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB, or other thermal surface. The internal power-dissipating components are mounted to the baseplate of the converter and all heat flow is through the baseplate. The lid of the converter does not provide a good thermal path.

The maximum temperature rise from junction to case is 20 °C at 9 A output and 15 °C at 6 A output.



## 6.5 RADIATION HARDNESS ASSURANCE

VPT takes a conservative approach to radiation testing to ensure product performance in a space environment. VPT's DLA-approved Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for guaranteeing the performance of VPT products under various environmental conditions in space including Total Ionizing Dose (TID) and Single-Event Effects (SEE). Additionally, Enhanced Low Dose-Rate Sensitivity (ELDRS) effects are considered for all bipolar ICs used in the hybrid. Hardness is guaranteed by a combination of both hybrid-level characterization and Radiation Lot Acceptance Testing (RLAT) of all sensitive semiconductor piece-parts used within the hybrid.

### 6.5.1 Radiation Test and Performance Levels

| Radiation Environment | | Piece Part RLAT | Hybrid-Level Characterization |
|---|---|---|---|
| Total Ionizing Dose (TID) | High Dose Rate (HDR) | 100 krad(Si) | 100 krad(Si) |
| | Low Dose Rate (LDR) | [1]50 krad(Si) | 100 krad(Si) |
| [2]Single-Event Effects (SEE) | Destructive (SEB, SEGR, SEL) | Not applicable | ≥ 85 MeV/mg/cm$^2$ |
| | Non-Destructive (SET, SEU) | Not applicable | ≥ 85 MeV/mg/cm$^2$ |
| [3]Displacement Damage (DD) | | 1x10$^{12}$ n/cm$^2$ | Not applicable |

1. The microcircuit device within the hybrid was characterized by its manufacturer to 150 krad(Si) at LDR and shown to be ELDRS free. Additionally, piece-part LDR radiation lot acceptance testing is performed to the level indicated.
2. The microcircuit device within the hybrid was characterized by its manufacturer for destructive SEE. Non-destructive SEE was tested by VPT during hybrid level characterization.
3. The microcircuit device was characterized per MIL-STD-883 Method 1017 to the level indicated. The device will be retested after design or process changes that may affect its RHA response.

### 6.5.2 RHA Plan Summary

| Test | RHA Plan for SV Series Isolated DC-DC Converters |
|---|---|
| Total Ionizing Dose (TID): | Sensitive semiconductor components undergo RLAT to 100 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 100 krad(Si). |
| Enhanced Low Dose Rate Sensitivity (ELDRS): | All bipolar linear ICs are characterized for ELDRS and tested in accordance with MIL-STD-883 test method 1019 section 3.13 |
| Single Event Effects (SEE): | Converters are characterized to LET ≥ 85 MeV/mg/cm$^2$ for both catastrophic events (SEL, SEB, SEGR) and functional interrupts (SEFI) under heavy ion exposure. Converters are also characterized for cross-section and magnitude of output transients (SET) for at least 3 different LET levels. |
| Radiation Lot Acceptance Testing (RLAT): | All production lots of sensitive semiconductor components undergo RLAT for TID at HDR and/or LDR as appropriate per part type. |
| Displacement Damage (DD): | The potentially sensitive microcircuit device is characterized to 1x1012 n/cm2 per MIL-STD-883 Method 1017. |

### 6.5.3 RHA Designators available on SMD

The SVPL1209S series converters are available on SMD with RHA level R. See section 8.0 for full SMD number information.

### 6.5.4 Supporting Documentation Available (Contact Sales)

| Report | Description |
|---|---|
| Radiation Hardness Assurance Plan: | DLA-approved RHA plan covering TID, SEE, and ELDRS |
| Worst-Case Analysis Report: | Detailed worst-case analysis including electrical stress/derating limits and guaranteed circuit performance post-radiation and end of life |
| Radiation Test Summary Report: | Overview of piece-part RLAT and hybrid characterization for all guaranteed environments. Also includes SEE cross-section data. |
| Reliability Report: | MTBF report based on MIL-HDBK-217 reliability calculations. |
| Thermal Analysis Report: | Component temperature rise analysis and measurement results. |

## 7.0 ENVIRONMENTAL SCREENING

100% tested per MIL-STD-883 as referenced to MIL-PRF-38534.

Contact sales for more information concerning additional environmental screening and testing options. VPT Inc. reserves the right to ship higher screened or SMD products to meet orders for lower screening levels at our sole discretion unless specifically forbidden by customer contract.

| Test | MIL-STD-883 Test Method, Condition | /H+ (Class H Screening + PIND) | /K and /KL1[1,7] (Class K Screening) | /EM (Engineering Model, Non-QML[1,6]) |
|---|---|---|---|---|
| Non-Destructive Bond Pull | TM2023 | •[2] | • | •[2] |
| Internal Visual | TM2010, TM2017, TM2032 (MIL-STD-750, TM2072, TM2073) | • | • | • |
| Temperature Cycling | TM1010, Condition C -65 °C to 150 °C, Ambient | • | • | |
| Constant Acceleration | TM2001, 3000g, Y1 Direction | • | • | |
| PIND[3] | TM2020, Condition A | •[2] | • | |
| Pre Burn-In Electrical | 25 °C | | • | |
| Burn-In | TM1015, 320 hrs., 125 °C, Case Typ | | • | |
| | TM1015, 160 hrs., 125 °C, Case Typ | • | | |
| | 24 hrs., 125 °C, Case Typ | | | • |
| Final Electrical | MIL-PRF-38534, Group A Subgroups 1-6 -55 °C, 25 °C, 125 °C[4] | • | • | |
| | MIL-PRF-38534, Group A Subgroups 1 and 4 25 °C | | | • |
| Hermeticity (Seal) | TM1014, Fine Leak, Condition A2 or B1 | • | • | |
| | TM1014, Gross Leak, Condition C1 or B2 | • | • | |
| | Gross Leak, Dip ($1x10^{-3}$) | | | • |
| Radiography[5] | TM2012 | | • | |
| External Visual | TM2009 | • | • | • |

1. Non-QML products may not meet all requirements of MIL-PRF-38534.
2. Not required per MIL-PRF-38534. Test performed for additional product quality assurance.
3. PIND test Certificate of Compliance included in product shipment.
4. 100% R&R testing with all test data included in product shipment.
5. Radiographic test Certificate of Compliance and film(s) or data CD included in product shipment.
6. Engineering models utilize only the screening specified and are not considered compliant for flight use.
7. -KL1 products are identical in every way with Class K products in compliance with MIL-PRF-38534 revision L and later revisions except they contain elements evaluated to the requirements of MIL-PRF-38534 revision K and previous revisions. These devices are not marked with an SMD number or MIL-PRF-38534 certification mark and are marked with -KL1 screening code in place of -K.

## 8.0 STANDARD MICROCIRCUIT DRAWING (SMD) NUMBERS

| Standard Microcircuit Drawing Number | SVPL1209S Series Similar Part Number |
|---|---|
| 5962R1723101HXC | SVPL1209S/H+ |
| 5962R1723101HXA | SVPL1209S/H+-E |
| 5962R1723101KXC | SVPL1209S/K |
| 5962R1723101KXA | SVPL1209S/K-E |

Do not use the SVPL1209S Series similar part number for SMD product acquisition. It is listed for reference only. For exact specifications of the SMD product, refer to the SMD drawing. SMDs can be downloaded from the DLA Land and Maritime (Previously known as DSCC) website at https://landandmaritimeapps.dla.mil/programs/defaultapps.asp. The SMD numbers listed above represents the Federal Stock Class, Device Type, Device Class Designator, Case Outline, Lead Finish and RHA Designator (where applicable). Please reference the SMD for other screening levels, lead finishes, and radiation levels. All SMD products are marked with a "Q" on the cover as specified by the QML certification mark requirement of MIL-PRF-38534.

## 9.0 ORDERING INFORMATION

| SVPL | 12 | 09 | S | /K | - | E |
|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | | 6 |

| (1) Product Series | (2) Nominal Input Voltage | (3) Output Current | (4) Number of Outputs | (5) Screening Code[1,2,3,4] | (6) Additional Screening Code |
|---|---|---|---|---|---|
| **SVPL** | **12** 12 Volts | **09** 9 Amps | **S** Single | **/EM** Engineering Model<br>**/H+** Class H + PIND<br>**/K** Class K<br>**/KL1** Class K (KL1) | Contact Sales |

1. Contact the VPT Sales Department for availability of Class H (/H), Class K (/K), or KL1 (/KL1) qualified products.
2. VPT Inc. reserves the right to ship higher screened or SMD products to meet lower screened orders at our sole discretion unless specifically forbidden by customer contract.
3. Engineering models utilize only the standard screening specified and are not considered compliant for flight use. These models are intended for low volume engineering characterization only and have no guarantee regarding operation in a radiation environment. The customer must place the following statement on each line item of their purchase order(s) for /EM units when ordering engineering models:

   "(Customer Name) acknowledges that the /EM unit listed in this line item is not permitted for flight use and will be used for Engineering characterization only."
4. -KL1 products are identical in every way with Class K products in compliance with MIL-PRF-38534 revision L and later revisions except they contain elements evaluated to the requirements of MIL-PRF-38534 revision K and previous revisions. These devices are not marked with an SMD number or MIL-PRF-38534 certification mark and are marked with -KL1 screening code in place of -K.

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, source inspection, and/or special element evaluation for space or other higher quality applications.

## 10.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

**Phone**: (425) 353-3010
**Fax**: (425) 353-4030
**E-mail**: vptsales@vptpower.com

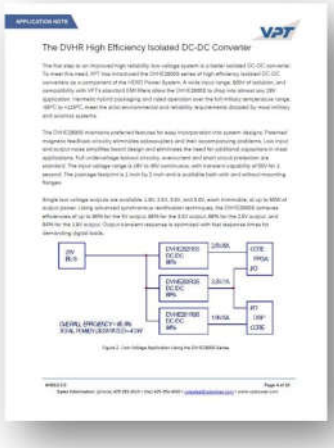
All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

## 11.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

**Product Catalogs**


**Application Notes and White Papers**

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