DATA SHEET

Power Your Critical Mission Today

SVFA0515SG SERIES

SPACE QUALIFIED POINT OF LOAD CONVERTERS

SVFA Series DC-DC Converter

Models Available
Input: 5V Nominal
15 A output
Qualified to MIL-PRF-38534 Class H and Class K

1.0 DESCRIPTION

The SVFA Series of space qualified point of load DC-DC converters is specifically designed for the harsh radiation environment of space applications. Performance is guaranteed through the use of hardened semiconductor components, radiation lot acceptance testing (RLAT) of non-hardened components, and analysis. The SVFA Series has been characterized for Total Ionizing Dose (TID) performance including Enhanced Low Dose Rate Sensitivity (ELDRS) and for Single Event Effects (SEE) according to VPT's DLA-approved Radiation Hardness Assurance (RHA) plan per MIL-PRF-38534, Appendix G, Level P. Characterization is performed at both the component level and at the SVFA hybrid converter level.

The SVFA Series of point of load DC-DC converters is radiation tolerant and suited for use in low Earth orbit (LEO), medium Earth orbit (MEO), geostationary orbit (GEO), deep space, and launch vehicle programs.

1.1 FEATURES

- Operates from 5 V input
- Adjustable Output from 0.8 to 3.4V
- Up to 15 Amps Output
- High Efficiency, up to 94%
- High Power Density, up to 150 W/in^3
- Output Inhibit Control
- Low Output Noise
- No Use of Optoisolators
- Short Circuit Protection

1.2 SPACE LEVEL CHARACTERIZATIONS

- Guaranteed TID performance to 40 krad(Si) including ELDRS.
- SEE performance to 85 MeV-cm^2/mg. Transients are fully characterized for cross section and magnitude.
- Worst-case analysis, stress, radiation, reliability reports available

1.3 MANUFACTURING AND COMPLIANCE

- Qualified to MIL-PRF-38534 Class H and Class K, DLA SMD # TBD
- MIL-PRF-38534 element evaluated components
- Manufactured in a MIL-PRF-38534 Class H and Class K facility
- MIL-STD-883
- ISO-9001

1.4 PACKAGING

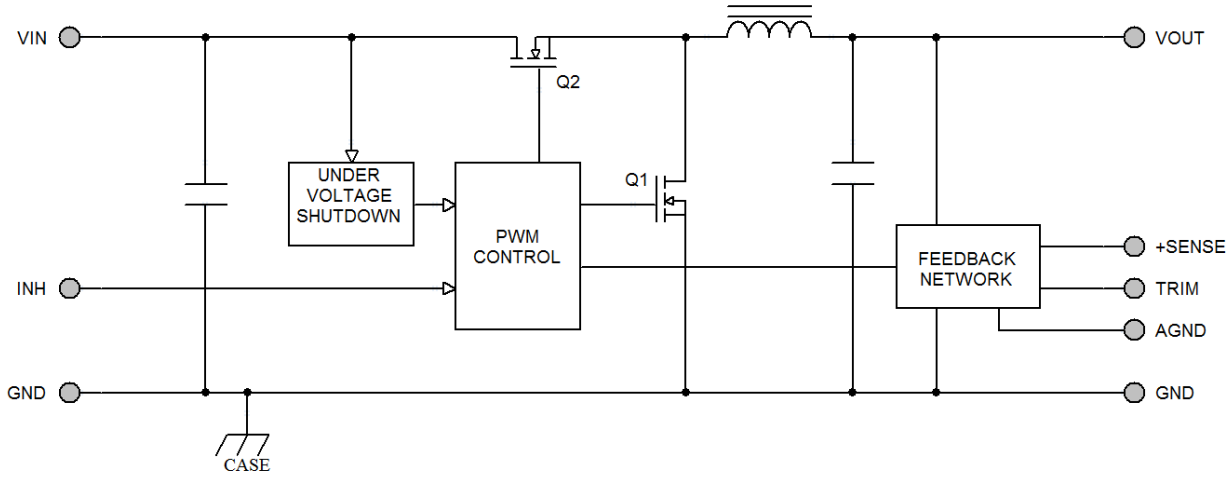
- Low-profile: 1.110" x 1.110" x 0.276"
- Max weight: 22 g
- Precision seam-sealed hermetic metal case

1.5 SIMILAR PRODUCTS AND ACCESSORIES

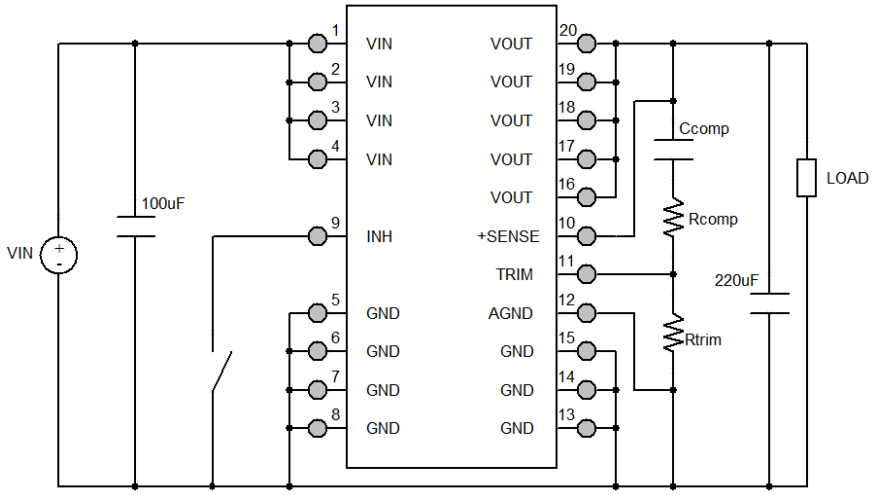
- SVFA0515S 15 A space qualified point of load DC-DC converter
- SVFA0510S 10 A space qualified point of load DC-DC converter
- SVFA0510SG 10 A space qualified point of load DC-DC converter
- SVGA0510SG 10 A space qualified point of load DC-DC converter
- SVGA0515SG 15 A space qualified point of load DC-DC converter
- SVRGA0508S 8 A space qualified point of load DC-DC converter
- Custom versions available
- Space qualified isolated DC-DC converters, 6 - 100 W

2.0 DIAGRAMS

2.1 BLOCK DIAGRAM



2.2 CONNECTION DIAGRAM



1. Rtrim should be connected directly across pins 11 and 12 as close as possible to the SVFA.
2. AGND should be connected to GND close to the SVFA. Voltage difference between the AGND and the GND pins greater than 0.3 V may result in regulation error and/or damage to the SVFA.
3. If not using INH, leave pin 9 open.
4. Rcomp and Ccomp are optional components that can be used to optimize the SVFA transient response.

3.0 SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings			
Input Voltage (Continuous):	-0.3 V to 7 V	Operating Temperature:	-55 °C to +125 °C
Input Voltage (Transient, 1 second):	-0.3 V to 7.5 V	Storage Temperature:	-65 °C to +150 °C
AGND	-0.3 V to 0.3 V	Lead Solder Temperature (10 seconds):	270 °C
ESD Rating per MIL-PRF-38534:	1C	Solder Reflow Temperature (30 seconds):	220 °C

3.2 PERFORMANCE SPECIFICATIONS[1]

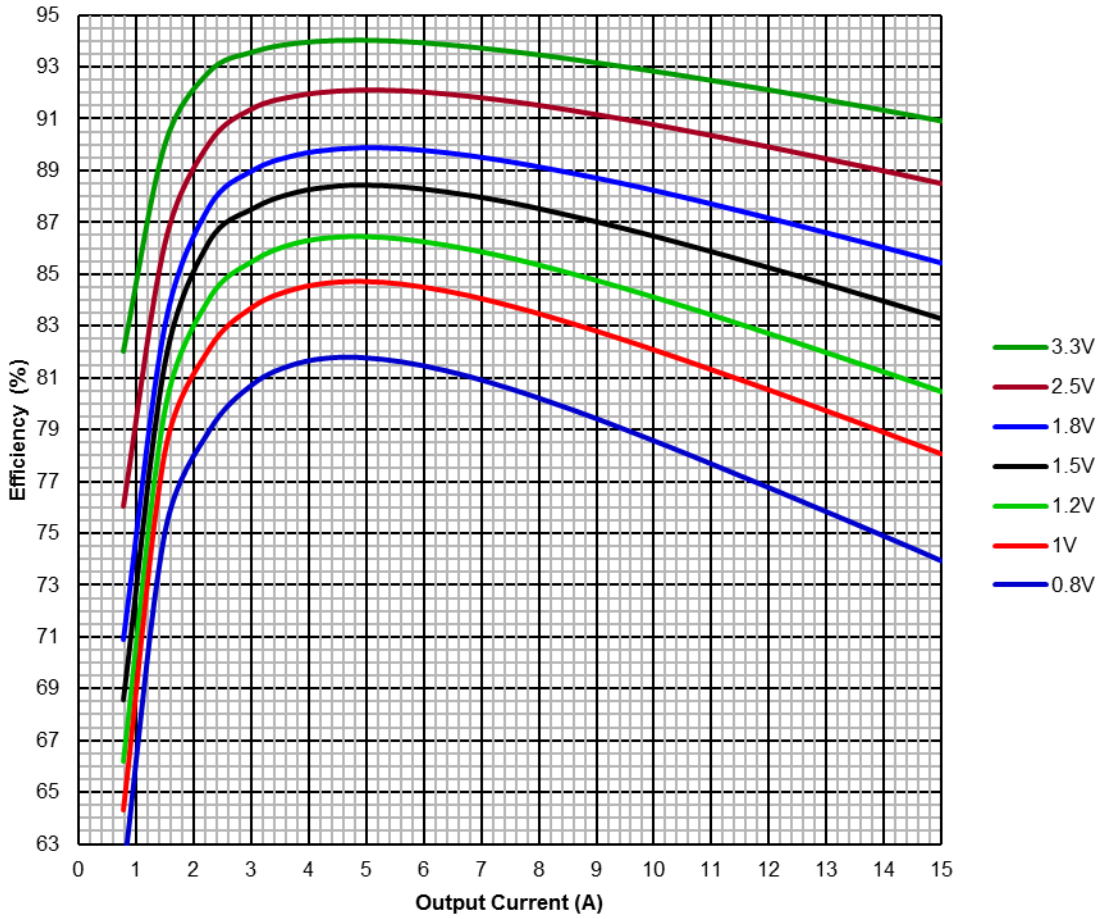
T_{CASE} = -55 °C to +125 °C, Vin = +5 V ± 1%, Full Load, Unless Otherwise Specified

		SVFA0515SG			
Parameter	**Conditions[1]**	**Min**	**Typ**	**Max**	**Units**
INPUT					
Voltage Range[2]	V_{OUT} = 0.8 V to 2.5 V	3.5	-	7	V
	V_{OUT} = 2.6 V to 3.3 V	4.2		7	
Current	INH < 1.5 V	-	30	35	mA
	No Load	-	130	220	mA
Undervoltage Lockout[2,3]	Turn-On	-	3.0	-	V
	Turn-off	-	2.7	-	V
OUTPUT STATIC					
Voltage Regulation	T_{CASE} = 25 °C	-1.0	-	+1.0	%Vout
	T_{CASE} = -55 °C to +125 °C	-1.5	-	+1.5	%Vout
Power[4]		0	-	51	W
Current		0	-	15	A
Ripple Voltage	20 Hz to 10 MHz	-	90	180	mVpp
Load Regulation		-	0	0.2	%
Short Circuit Power Dissipation	V_{OUT} = 3.3 V prior to short circuit	-	2.5	5	W
OUTPUT DYNAMIC					
Load Step, Half to Full Load, V_{OUT} = 3.3 V	Output Transient	-	110	200	mV
	Recovery[5]	-	40	75	µs
Turn-On, V_{IN} = 0 to 5V	Delay	-	7.5	12	ms
	Overshoot	-	1	15	mVpk
FUNCTION					
INH Pin Input[2]	Output Inhibited	0	-	1.5	V
INH Pin Open Circuit Voltage[2]	Output Enabled	-	4.7	V_{IN}	V
GENERAL					
Efficiency	Vout = 3.3 V	86	91	-	%
Capacitive Load[2]		-	-	5000	µF
Switching Frequency		200	250	315	kHz
Weight	Standard package option	-	-	22	g
MTBF (MIL-HDBK-217F)	SF @ Tcase = 55 °C	-	6.64	-	MHr
POST-RAD END-OF-LIFE LIMITS[6]					
OUTPUT Voltage	T_{CASE} = -55 °C to +125 °C	-3.0	-	+3.0	%Vout
Switching Frequency	T_{CASE} = -55 °C to +125 °C, V_{IN} = 5 V	190	-	325	kHz
	T_{CASE} = -55 °C to +125 °C, V_{IN} = 3.6 to 7 V	185	-	350	kHz

1. Performance specifications are guaranteed with 100µF from VIN to GND.
2. Verified by qualification testing.
3. Output voltage not necessarily in regulation.
4. Dependent on output voltage.
5. Time for output voltage to settle within 1% of steady-state value.
6. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted.

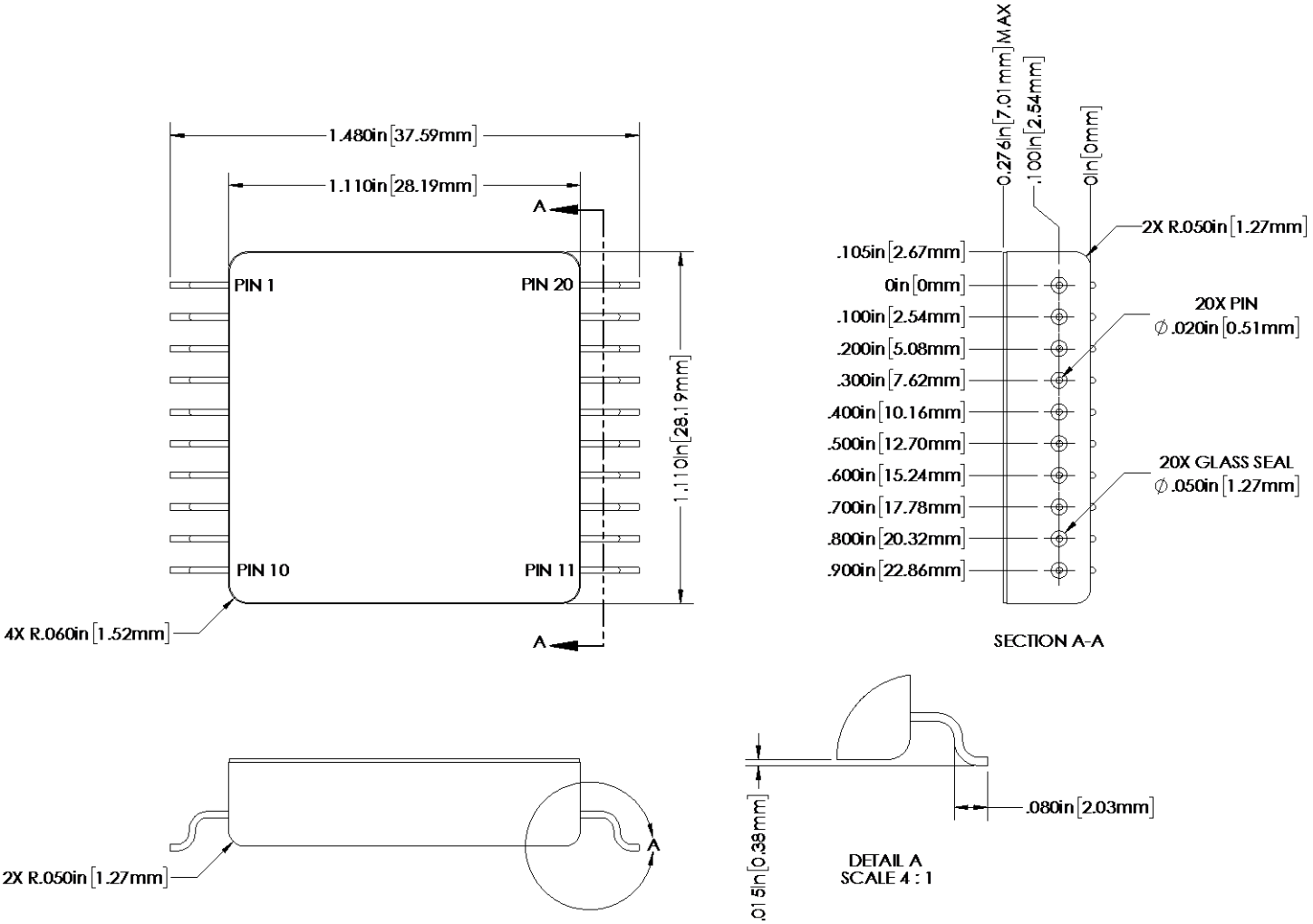
4.0 EFFICIENCY CURVES

4.1.1 SVFA0515SG Efficiency (Typical, 25 °C, Vin = 5V)



5.0 MECHANICAL OUTLINES AND PINOUT

Standard Package Option:

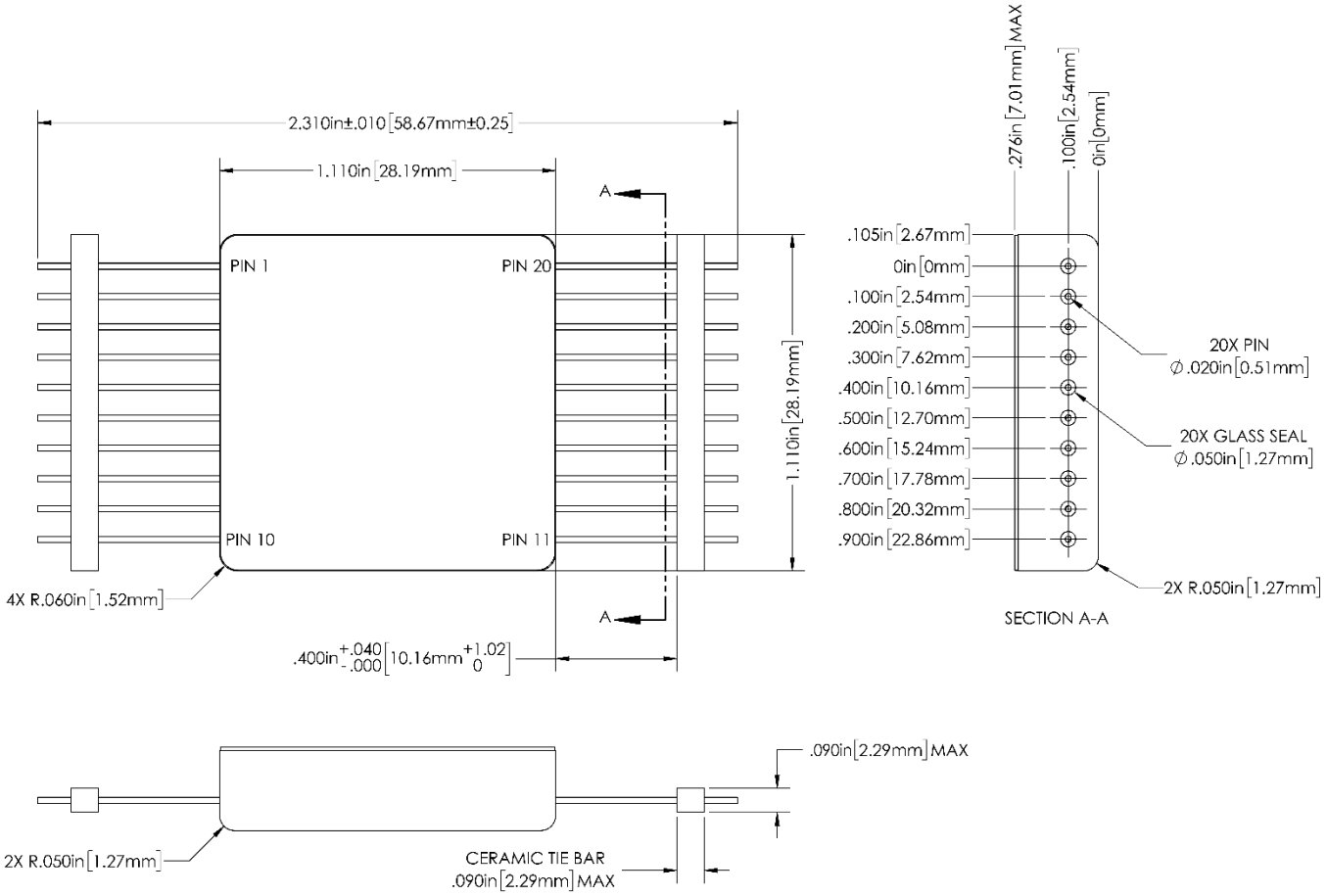


1. Tolerances are +0.005" unless otherwise stated
2. Case temperature is measured on the center of the baseplate surface
3. Materials: Case (Steel, gold over nickel plated); Cover (Kovar, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated, 63/37 SnPb solder dipped); Pin Seals (Glass)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VIN	6	GND	11	TRIM	16	VOUT
2	VIN	7	GND	12	AGND	17	VOUT
3	VIN	8	GND	13	GND	18	VOUT
4	VIN	9	INH	14	GND	19	VOUT
5	GND	10	+SENSE	15	GND	20	VOUT

5.0 MECHANICAL OUTLINES AND PINOUT (CONTINUED)

Optional Straight-Lead Package:



1. Tolerances are +0.005" unless otherwise stated
2. Case temperature is measured on the center of the baseplate surface
3. Materials: Case (Steel, gold over nickel plated); Cover (Kovar, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated); Pin Seals (Glass)
4. Pins may have exposed nickel plating (not base metal) beyond the ceramic tie bars due to the plating process. No nickel plating is exposed between the tie bar and case.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VIN	6	GND	11	TRIM	16	VOUT
2	VIN	7	GND	12	AGND	17	VOUT
3	VIN	8	GND	13	GND	18	VOUT
4	VIN	9	INH	14	GND	19	VOUT
5	GND	10	+SENSE	15	GND	20	VOUT

6.0 TECHNICAL NOTES

Please note that many of these functions are also demonstrated in detail on the VPT website in the form of technical video labs.

6.1 GENERAL INFORMATION

6.1.1 Topology Description

The SVFA0515SG is a non-isolated, fixed-frequency, radiation-hardened, synchronous buck converter. It operates from a 5 V input and provides a stepped-down, precisely regulated, programmable output voltage at high efficiency. The SVFA0515SG is optimized for low voltage point-of-load (POL) applications.

6.1.2 External Components

The SVFA0515SG Series has internal input and output capacitors. To meet the performance specifications in Section 3.2, a minimum additional 100 µF tantalum input decoupling capacitor is required. The SVFA0515SG is stable with no load capacitance. Additional output capacitance is allowed up to the maximum listed in Section 3.2.

6.1.3 Source Impedance

The impedance of the 5V input source can interact with the POL converter and can affect performance. High source impedance is often caused by a long input cable or other components added in series with the input. In some cases, additional input capacitance will be needed to stabilize the system.

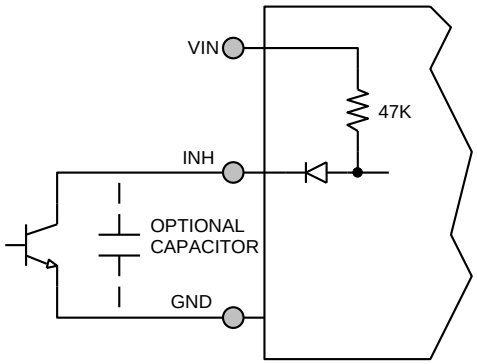
6.1.4 Case Connection

The SVFA0515SG case is connected to GND at a single point inside of the package.

6.2 FUNCTION DESCRIPTIONS

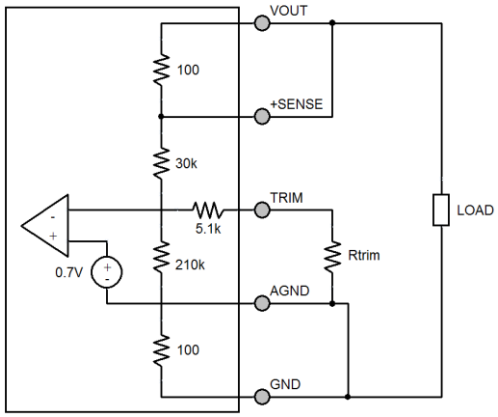
6.2.1 On/Off Control (Inhibit)

The INH (Inhibit) pin is a control pin referenced to GND. The INH pin must be driven using an open-collector or open-drain configuration. Pulling the INH pin low disables the converter output. Leaving INH open enables the output, allowing the converter to operate normally. The pin must be pulled below 1.5V to disable the output. An optional capacitor from INH to GND may be used to delay turn-on. The INH pin should be left open if not used.



6.2.2 Adjusting the Output Voltage (TRIM)

The output voltage of the converter is set with an external resistor connected from the TRIM pin to the AGND pin. Use the equations or table below to choose the trim resistor value. Trim resistor tolerance of 0.1% is recommended to achieve an accurate output voltage. The default output voltage with the TRIM pin left open is 0.8 V.



$$R_{trim} = \frac{21000}{V_{OUT} - 0.8} - 5100$$

$$V_{OUT} = \frac{21000}{R_{TRIM} + 5100} + 0.8$$

SVFA0515SG	
+Vout (V)	**Rtrim (Ω)**
0.8	Open
0.9	205k
1.0	99.9k
1.2	47.4k
1.5	24.9k
1.8	15.9k
2.0	12.4k
2.5	7.25k
2.8	5.40k
3.0	4.44k
3.3	3.30k
3.4	2.98k

6.2.3 Output Capacitors

Output capacitors for point-of-load (POL) DC/DC converters should be chosen to meet output voltage ripple and transient requirements. Meeting the transient response requirement is accomplished by making the output impedance of the converter sufficiently small. Given the high control bandwidth of POL converters like the SVFA series, the peak output impedance is typically dominated by the equivalent series resistance (ESR) of the bulk output capacitance. Therefore, the output capacitors should be chosen to set a certain maximum total ESR. The total ESR is the parallel combination of the internal bulk capacitor's ESR and that of the added capacitors. Given the output voltage transient requirement, maximum load step, and the ESR of each bulk capacitor that will be added, the number of added capacitors needed is calculated with the following equations:

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}}$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}}$$

Parameter	Definition
ΔV_{OUT}	Max V_{OUT} transient allowed
ΔI_{OUT}	Max load current step
ESR_{TOTAL}	Total combined parallel ESR, including internal and added capacitors
ESR_{ADDED}	Combined parallel ESR of the added capacitors
$ESR_{INTERNAL}$	ESR of the internal bulk capacitor (**43.7mΩ max** under worst-case conditions)
ESR_{EACH}	ESR of each of the added capacitors
N	Number of added capacitors

For example, assume that V_{OUT} is 1.5 V, the maximum output transient allowed is 37.5mV, and the load step is 4.5 A. Assume the output capacitors being used are 330 µF and have a maximum ESR of 50 mΩ each.

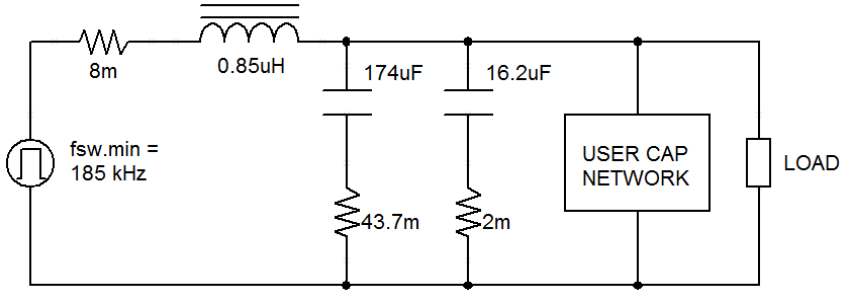
$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{37.5mV}{4.5A} = 8.33m\Omega$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}} = \frac{8.33m\Omega * 43.7m\Omega}{43.7m\Omega - 8.33m\Omega} = 10.30m\Omega$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}} = \frac{50m\Omega}{10.30m\Omega} = 4.85 \rightarrow use\ 5\ output\ capacitors$$

In the example, 5x 330 µF/50 mΩ capacitors are needed. This is a total capacitance of 1650 µF, which is well below the 5000 µF maximum allowed.

The output voltage ripple can be evaluated through simulation using the circuit below. This circuit incorporates worst-case conditions that include the effects of component tolerances, temperature extremes (-55 °C to 125 °C), radiation (40 krad), and aging (10 year mission). Note that the resistor shown in series with the inductor includes the resistance of the inductor and power FETs. The pulsed voltage source should have a peak voltage equal to the input voltage and the minimum switching frequency (185 kHz) to evaluate the worst-case ripple. The duty cycle should be adjusted to attain the correct output voltage.



6.3 PROTECTION FEATURES

6.3.1 Input Undervoltage Lockout

The SVFA0515SG Series provides input undervoltage lockout protection. For input voltages below the turn-on voltage, the converter will remain off. When the input voltage exceeds the turn-on voltage, the converter will start. For input voltages below the operating range of the converter but above the UVLO turn-off voltage, the converter may reach its maximum duty cycle and the output may be out of regulation.

6.3.2 Output Soft-Start

The SVFA0515SG Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately 3 ms. The soft-start function is active whether the module is turned on with an application of input voltage or from release of the INH pin. The turn-on delay time is specified from the application of input voltage (or release of INH pin) until the output reaches 90% of its final value.

6.3.3 Output Short Circuit Protection

The SVFA0515SG Series provides output short circuit protection. When a sustained high peak current is detected, the converter will shut down and enter a hiccup mode. After a delay, the converter will attempt a soft-start. This sequence will continue until the fault is removed, allowing the converter to soft-start and resume normal operation.

6.4 THERMAL CONSIDERATIONS

The SVFA0515SG is rated for full power operation at 125 °C. Above 125 °C, the output power must be derated linearly from full power at 125 °C to zero power at 135 °C. The operating temperature of the converter is specified on the baseplate of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB, or other thermal surface. The internal power-dissipating components are mounted to the baseplate of the converter and all heat flow is through the baseplate. The lid of the converter does not provide a good thermal path.

The maximum temperature rise from junction to case is 14 °C at full load.

6.5 RADIATION HARDNESS ASSURANCE

VPT takes a conservative approach to radiation testing to ensure product performance in a space environment. VPT's DLA-approved Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for guaranteeing the performance of VPT products under various environmental conditions in space including Total Ionizing Dose (TID) and Single-Event Effects (SEE). Additionally, Enhanced Low Dose-Rate Sensitivity (ELDRS) effects are considered for all bipolar ICs used in the hybrid. Hardness is guaranteed by a combination of both hybrid-level characterization and Radiation Lot Acceptance Testing (RLAT) of all sensitive semiconductor piece-parts used within the hybrid.

6.5.1 Radiation Test and Performance Levels

Radiation Environment		Piece Part RLAT	Hybrid-Level Characterization
Total Ionizing Dose (TID)	High Dose Rate (HDR)	40 krad(Si)	40 krad(Si)
	Low Dose Rate (LDR)	[1]40 krad(Si)	40 krad(Si)
Single-Event Effects (SEE)	Destructive (SEB, SEGR, SEL)	Not applicable	≥ 85 MeV/mg/cm^2
	Non-Destructive (SET, SEU)	Not applicable	≥ 85 MeV/mg/cm^2
Displacement Damage (DD)		1x10^{12} n/cm^2	Not applicable

1. Piece-part LDR screening performed only on potentially ELDRS parts (bipolar ICs).

6.5.2 RHA Plan Summary

Test	RHA Plan for SVL Series Isolated DC-DC Converters
Total Ionizing Dose (TID):	Sensitive semiconductor components undergo RLAT to 40 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 40 krad(Si).
Enhanced Low Dose Rate Sensitivity (ELDRS):	All bipolar linear ICs are characterized for ELDRS and tested in accordance with MIL-STD-883 test method 1019 section 3.13
Single Event Effects (SEE):	Converters are characterized to LET ≥ 85 MeV/mg/cm^2 for both catastrophic events (SEL, SEB, SEGR) and functional interrupts (SEFI) under heavy ion exposure. Converters are also characterized for cross-section and magnitude of output transients (SET) for at least 3 different LET levels.
Radiation Lot Acceptance Testing (RLAT):	All production lots of sensitive semiconductor components undergo RLAT for TID at HDR and/or LDR as appropriate per part type.
Displacement Damage (DD):	Sensitive semiconductor components undergo RLAT to 1x10^{12} n/cm^2 per MIL-STD-883 Method 1017.

6.5.3 RHA Designators available on SMD

The SVFA0515SG series converters are available on SMD with RHA level P. See section 8.0 for full SMD number information.

6.5.4 Supporting Documentation Available (Contact Sales)

- Radiation Hardness Assurance Plan: DLA-approved RHA plan covering TID, SEE, and ELDRS
- Worst-Case Analysis Report: Detailed worst-case analysis including electrical stress/derating limits and guaranteed circuit performance post-radiation and end of life
- Radiation Test Summary Report: Overview of piece-part RLAT and hybrid characterization for all guaranteed environments. Also includes SEE cross-section data.
- Reliability Report: MTBF report based on MIL-HDBK-217 reliability calculations.
- Thermal Analysis Report: Component temperature rise analysis and measurement results.

7.0 ENVIRONMENTAL SCREENING

100% tested per MIL-STD-883 as referenced to MIL-PRF-38534.

Contact sales for more information concerning additional environmental screening and testing options. VPT Inc. reserves the right to ship higher screened or SMD products to meet orders for lower screening levels at our sole discretion unless specifically forbidden by customer contract.

Test	MIL-STD-883 Test Method, Condition	/H+ (Class H + PIND)	/K (Class K)	/EM (Engineering Model) Non-QML[1,6]
Non-Destructive Bond Pull	TM2023	•[2]	•	•[2]
Internal Visual	TM2010, TM2017, TM2032 (MIL-STD-750, TM2072, TM2073)	•	•	•
Temperature Cycling	TM1010, Condition C -65 °C to 150 °C, Ambient	•	•	
Constant Acceleration	TM2001, 3000g, Y1 Direction	•	•	
PIND[3]	TM2020, Condition A	•[2]	•	
Pre Burn-In Electrical	25 °C		•	
Burn-In	TM1015, 320 hrs., 125 °C, Case Typ		•	
	TM1015, 160 hrs., 125 °C, Case Typ	•		
	24 hrs., 125 °C, Case Typ			•
Final Electrical	MIL-PRF-38534, Group A Subgroups 1-6 -55 °C, 25 °C, 125 °C[4]	•	•	
	MIL-PRF-38534, Group A Subgroups 1 and 4 25 °C			•
Hermeticity (Seal)	TM1014, Fine Leak, Condition A2 or B1	•	•	
	TM1014, Gross Leak, Condition C1 or B2	•	•	
	Gross Leak, Dip ($1x10^{-3}$)			•
Radiography[5]	TM2012		•	
External Visual	TM2009	•	•	•

1. Non-QML products may not meet all requirements of MIL-PRF-38534
2. Not required per MIL-PRF-38534. Test performed for additional product quality assurance
3. PIND test Certificate of Compliance included in product shipment
4. 100% R&R testing with all test data included in product shipment
5. Radiographic test Certificate of Compliance and film(s) or data CD included in product shipment
6. Engineering models utilize only the screening specified and are not considered compliant for flight use

8.0 STANDARD MICROCIRCUIT DRAWING (SMD) NUMBERS

Standard Microcircuit Drawing Number	SVFA0515SG Series Similar Part Number
TBD	SVFA0515SG/H+ SVFA0515SG/H+-E SVFA0515SG/K SVFA0515SG/K-E

Do not use the SVFA0515SG Series similar part number for SMD product acquisition. It is listed for reference only. For exact specifications for the SMD product, refer to the SMD drawing. SMDs can be downloaded from the DLA Land and Maritime (Previously known as DSCC) website at https://landandmaritimeapps.dla.mil/programs/defaultapps.asp. The SMD number listed above is for standard gold-plated lead finish and "R" RHA (Radiation Hardness Assurance) level. Please reference the SMD for other screening levels, lead finishes, and radiation levels. All SMD products are marked with a "Q" on the cover as specified by the QML certification mark requirement of MIL-PRF-38534.

9.0 ORDERING INFORMATION

SVFA	05	15	S	G		/K	-	E
1	2	3	4	5	6	7		8

(1) Product Series	(2) Nominal Input Voltage	(3) Output Current	(4) Number of Outputs	(5) Package Option	(6) Package Lead Option[4]	(7) Screening Code[1,2,3]	(8) Additional Screening Code[4]
SVFA	**05** 5 Volts	**15** 15 Amps	**S** Single	**G** Gullwing	**None** Formed **N** Straight	**/EM** Engineering Model **/H+** Class H + PIND **/K** Class K	**E** Solder Dipped Contact Sales for additional options

1 Contact the VPT Sales Department for availability of Class H (/H) or Class K (/K) qualified products
2 VPT Inc. reserves the right to ship higher screened or SMD products to meet lower screened orders at our sole discretion unless specifically forbidden by customer contract
3 Engineering models utilize only the standard screening specified and are not considered compliant for flight use. These models are intended for low volume engineering characterization only and have no guarantee regarding operation in a radiation environment. The customer must place the following statement on each line item of their purchase order(s) for /EM units when ordering engineering models:

"(Customer Name) acknowledges that the /EM unit listed in this line item is not permitted for flight use and will be used for Engineering characterization only."

4 When selecting Package Lead Option "Formed", Additional Screening Code "-E" (solder dipped leads) must also be applied. When selecting Package Lead Option "Straight", Additional Screening Code "-E" should not be applied.

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, source inspection, and/or special element evaluation for space or other higher quality applications.

10.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

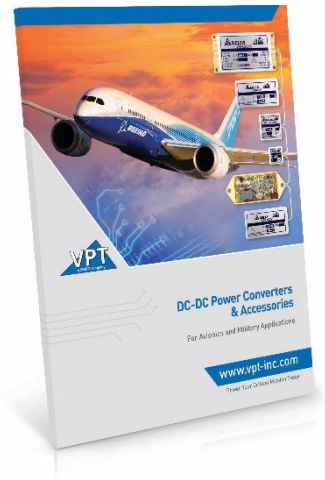
Phone: (425) 353-3010
Fax: (425) 353-4030
E-mail: vptsales@vptpower.com

All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

11.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

Product Catalogs



Application Notes and White Papers

Technical Video Labs

Additional Products For Avionics/Military, Hi-Rel COTS, and Space Applications