



Power Your Critical Mission Today

SVRFL2800D SERIES

SPACE QUALIFIED HYBRID DC-DC CONVERTERS



SVRFL Series DC-DC Converter

Models Available

 Input: 18 V to 40 V continuous, 50 V transient

 100 W, dual outputs of ± 5 V, ± 12 V, ± 15 V

 Qualified to MIL-PRF-38534 Class H and Class K

 Designed for TOR Compliance

1.0 DESCRIPTION

The SVRFL Series of space qualified DC-DC converters is specifically designed for the harsh radiation environment of space applications and is designed in accordance with Aerospace TOR requirements. Performance is guaranteed through the use of hardened semiconductor components, radiation lot acceptance testing (RLAT) of non-hardened components, and analysis. The SVRFL Series has been characterized for Total Ionizing Dose (TID) performance including Enhanced Low Dose Rate Sensitivity (ELDRS) and for Single Event Effects (SEE) according to VPT's DLA-approved Radiation Hardness Assurance (RHA) plan per MIL-PRF-38534, Appendix G, Level R. Characterization is performed at both the component level and at the SVRFL Series hybrid converter level.

The SVRFL Series of DC-DC converters is radiation hardened and suited for use in low Earth orbit (LEO), medium Earth orbit (MEO), geostationary orbit (GEO), deep space, and launch vehicle programs.

1.1 FEATURES

- Up to 100 W output power
- Wide input voltage range: 18 V to 40 V plus 50 V transient
- Continuous operation over full military temperature range of -55 °C to +125 °C with no power derating
- Very low output noise
- Parallel up to 5 units with current sharing
- Output voltage trim up +10% or down -20%
- Radiation immune magnetic feedback circuit
- No use of optoisolators
- Undervoltage lockout
- Current limit protection / short circuit protection

Products and reports described in this datasheet are subject to all export license restrictions and regulations which may include but are not limited to ITAR (International Traffic in Arms Regulations) and the Export Administration and Foreign Assets Control Regulations. Further restrictions may apply. Contact VPT sales for details.

1.2 SPACE LEVEL CHARACTERIZATIONS

- Guaranteed TID performance to 100 krad(Si) including ELDRS
- SEE performance to 85 MeV/mg/cm². Transients are fully characterized for cross section and magnitude.
- Worst-case analysis, stress, radiation, reliability reports available

1.3 MANUFACTURING AND COMPLIANCE

- Qualified to MIL-PRF-38534 Class H and Class K, DLA SMD # 5962-13234
- Available compliant to MIL-HDBK-1547 and Aerospace TOR component level element evaluation
- MIL-PRF-38534 element evaluated components
- MIL-STD-461 C/D/E/F when used with appropriate VPT EMI filter
- Manufactured in a MIL-PRF-38534 Class H and Class K facility
- MIL-STD-883
- ISO-9001

1.4 PACKAGING

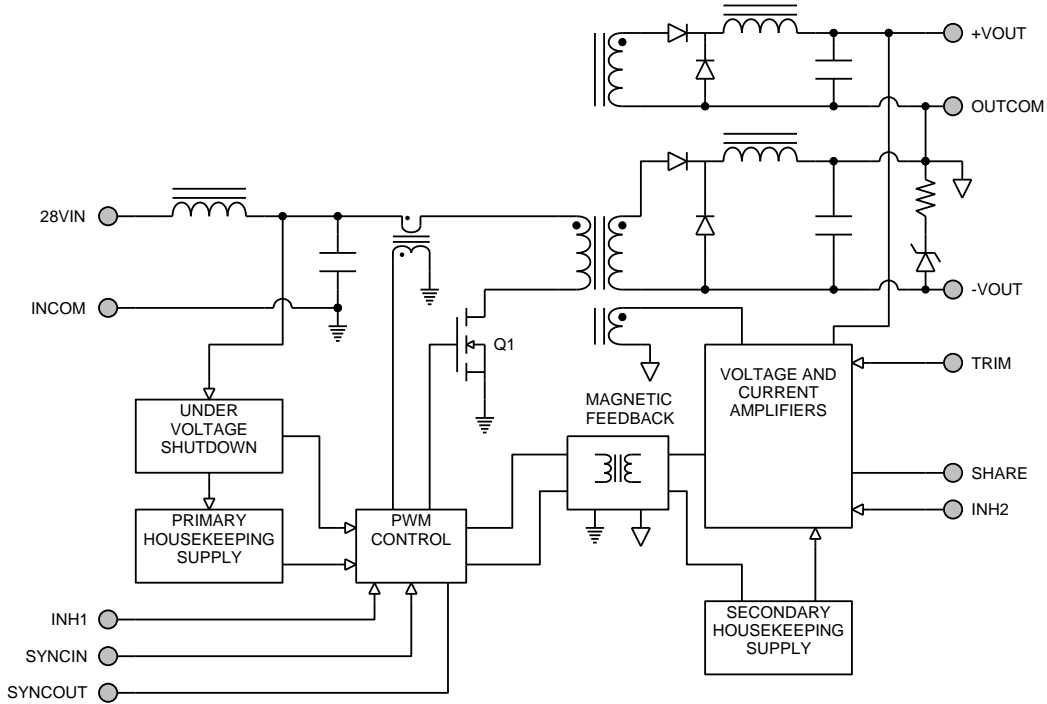
- Low-profile: 3.005" x 1.505" x 0.400"
- Max weight: 88 g
- Industry standard pinout
- Precision seam-welded hermetic metal case

1.5 SIMILAR PRODUCTS AND ACCESSORIES

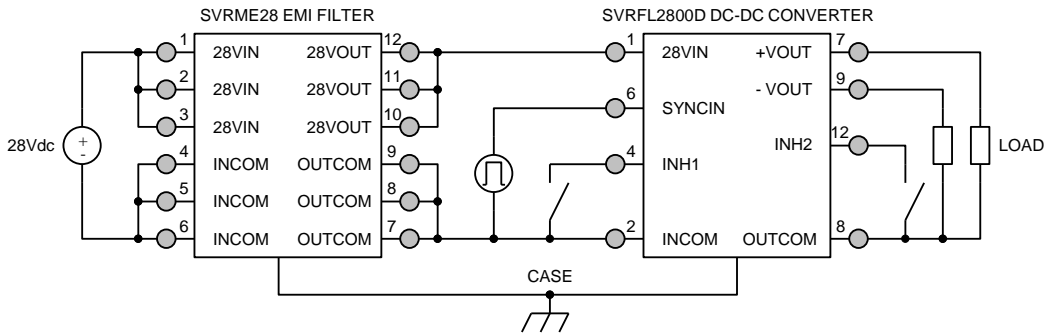
- [SVRFL](#) 100 W single output DC-DC converter
- [SVFL](#) 100 W space qualified DC-DC converter, 30 krad(Si)
- Custom versions available
- [EMI filters](#)
- Non-isolated, space qualified [point of load converters](#)
- Use with Thermal Pad [TP-001](#)

2.0 DIAGRAMS

2.1 BLOCK DIAGRAM



2.2 CONNECTION DIAGRAM



3.0 SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings			
Input Voltage (Continuous):	-0.5 V to 40 V	Operating Temperature (Full Load):	-55 °C to +125 °C
Input Voltage (Transient, 1 second):	-0.5 V to 50 V	Storage Temperature:	-65 °C to +150 °C
ESD Rating per MIL-PRF-38534:	3A	Lead Solder Temperature (10 seconds):	270 °C

3.2 PERFORMANCE SPECIFICATIONS

Tcase = -55 °C to +125 °C, Vin = +28 V ± 5%, Full Load¹, Unless Otherwise Specified

Parameter	Conditions ⁵	SVRFL2805D			SVRFL2812D			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
Voltage	Continuous	18	28	40 ⁷	18	28	40 ⁷	V
	Transient, 1 sec ⁴	-	-	50	-	-	50	V
Current	INH 1 < 1.5 V	-	3.5	8	-	3.5	8	mA
	INH 2 < 1 V	-	30	70	-	30	70	mA
	No Load	-	70	140	-	80	160	mA
Ripple Current	20 Hz to 10 MHz	-	60	160	-	60	160	mApp
Undervoltage Lockout	Turn-On	14.5	16	17.5	14.5	16	17.5	V
	Turn-Off ⁴	13	15	17	13	15	17	V
OUTPUT STATIC								
Voltage	+Vout, Tcase = 25 °C	4.95	5	5.05	11.88	12	12.12	V
	+Vout, Tcase = -55 °C to +125 °C	4.9	5	5.1	11.7	12	12.3	V
	-Vout, Tcase = 25 °C	4.8	5	5.2	11.8	12	12.2	V
	-Vout, Tcase = -55 °C to +125 °C	4.7	5	5.3	11.4	12	12.6	V
Power ²	Total	0	-	100	0	-	100	W
	Either Output	0	-	60	0	-	60	W
Current ²	Total	0	-	20	0	-	8.33	A
	Either Output	0	-	12	0	-	5	A
Ripple Voltage	20 Hz to 10 MHz	-	25	80	-	70	160	mVpp
Line Regulation	+Vout, VIN = 18 V to 40 V	-	2	20	-	1	20	mV
	-Vout, VIN = 18 V to 40 V	-	10	200	-	10	200	mV
Load Regulation ⁸	+Vout, No Load to Full Load	-	10	100	-	4	120	mV
	-Vout, No Load to Full Load	-	100	200	-	80	200	mV
Cross Regulation, -Vout	+Vout: 40% load, -Vout: 60% load	-	150	450	-	100	450	mV
	+Vout: 60% load, -Vout: 40% load	-	-	-	-	-	-	-
Load Fault Power Dissipation	Overload ⁴	-	-	50	-	-	50	W
	Short Circuit	-	-	50	-	-	50	W
OUTPUT DYNAMIC								
Load Step, Half to Full Load, Either Output	Output Transient	-	200	600	-	280	600	mVpk
	Recovery ³	-	230	500	-	200	500	µs
Line Step ⁴ , Vin = 18V to 40 V	Output Transient	-	150	600	-	250	800	mVpk
	Recovery ³	-	150	500	-	150	500	µs
Turn-On, Vin = 0 to 28 V	Delay	-	5	20	-	5	20	ms
	Overshoot	-	2	25	-	20	50	mVpk
FUNCTION								
INH 1 Pin Input ⁴	Output Inhibited	0	-	1.5	0	-	1.5	V
INH 2 Pin Input ⁴	Output Inhibited	0	-	1	0	-	1	V
INH 1 Pin Open Circuit Voltage ⁴	Output Enabled	9	-	15	9	-	15	V
INH 2 Pin Open Circuit Voltage ⁴	Output Enabled	4	-	12	4	-	12	V
Voltage Trim Range		-20	-	10	-20	-	10	%
SHARE Pin Voltage ⁴		2	-	4	2	-	4	V
SYNC Frequency Range		500	-	600	500	-	600	kHz
GENERAL								
Efficiency		75	80	-	80	86	-	%
Capacitive Load ⁴		-	-	500	-	-	300	µF
Switching Frequency		450	525	550	450	525	550	kHz
Isolation	500 V DC, Tcase = 25 °C	100	-	-	100	-	-	MΩ
Weight	Standard package option	-	-	88	-	-	88	g
MTBF (MIL-HDBK-217F) ⁶	SF, Class K @ Tcase = 55 °C	-	2.47	-	-	2.47	-	MHr

1. Half load at +Vout and half load at -Vout
2. Up to 60% of the total power or current can be drawn from either of the two outputs
3. Time for output voltage to settle within 1% of steady-state value
4. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified

5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted
6. Correction factor of 0.12 added to ceramic capacitors
7. 37.5 V Max continuous to be compliant to MIL-HDBK-1547 and Aerospace TOR
8. 5% load to full load at -55 °C

3.2 PERFORMANCE SPECIFICATIONS (CONTINUED)

Tcase = -55 °C to +125 °C, Vin = +28 V ± 5%, Full Load¹, Unless Otherwise Specified

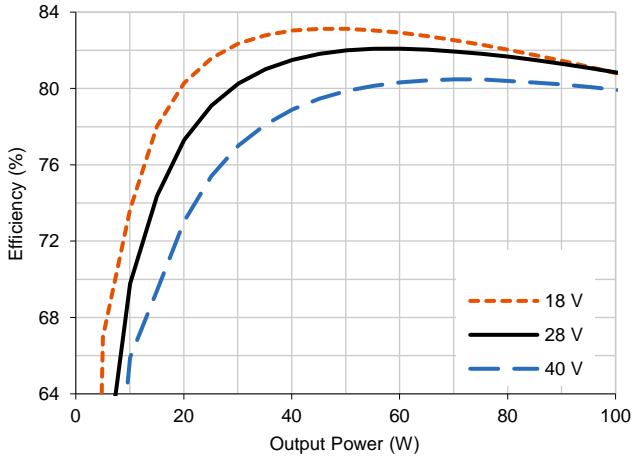
		SVRFL2815D			
Parameter	Conditions ⁵	Min	Typ	Max	Units
INPUT					
Voltage	Continuous	18	28	40 ⁷	V
	Transient, 1 sec ⁴	-	-	50	V
Current	INH 1 < 1.5 V	-	3.5	8	mA
	INH 2 < 1 V	-	30	70	mA
	No Load	-	100	160	mA
Ripple Current	20 Hz to 10 MHz	-	50	160	mApp
Undervoltage Lockout	Turn-On	14.5	16	17.5	V
	Turn-Off ⁴	13	15	17	V
OUTPUT STATIC					
Voltage	+Vout, Tcase = 25 °C	14.85	15	15.15	V
	+Vout, Tcase = -55 °C to +125 °C	14.625	15	15.375	V
	-Vout, Tcase = 25 °C	14.7	15	15.3	V
	-Vout, Tcase = -55 °C to +125 °C	14.275	15	15.725	V
Power ²	Total	0	-	100	W
	Either Output	0	-	60	W
Current ²	Total	0	-	6.67	A
	Either Output	0	-	4	A
Ripple Voltage	20 Hz to 10 MHz	-	80	160	mVpp
Line Regulation	+Vout, VIN = 18 V to 40 V	-	1	20	mV
	-Vout, VIN = 18 V to 40 V	-	15	200	mV
Load Regulation ⁸	+Vout, No Load to Full Load	-	5	120	mV
	-Vout, No Load to Full Load	-	50	200	mV
Cross Regulation, -Vout	+Vout: 40% load, -Vout: 60% load	-	80	450	mV
	+Vout: 60% load, -Vout: 40% load	-	80	450	mV
Load Fault Power Dissipation	Overload ⁴	-	-	50	W
	Short Circuit	-	-	50	W
OUTPUT DYNAMIC					
Load Step, Half to Full Load, Either Output	Output Transient	-	250	600	mVpk
	Recovery ³	-	150	500	µs
Line Step ⁴ , Vin = 18V to 40 V	Output Transient	-	500	1200	mVpk
	Recovery ³	-	200	500	µs
Turn-On, Vin = 0 to 28 V	Delay	-	5	20	ms
	Overshoot	-	20	50	mVpk
FUNCTION					
INH 1 Pin Input ⁴	Output Inhibited	0	-	1.5	V
INH 2 Pin Input ⁴	Output Inhibited	0	-	1	V
INH 1 Pin Open Circuit Voltage ⁴	Output Enabled	9	-	15	V
INH 2 Pin Open Circuit Voltage ⁴	Output Enabled	4	-	12	V
Voltage Trim Range		-20	-	10	%
SHARE Pin Voltage ⁴		2	-	4	V
SYNC Frequency Range		500	-	600	kHz
GENERAL					
Efficiency		75	83	-	%
Capacitive Load ⁴		-	-	300	µF
Switching Frequency		450	550	550	kHz
Isolation	500 V DC, Tcase = 25 °C	100	-	-	MΩ
Weight	Standard package option	-	-	88	g
MTBF (MIL-HDBK-217F) ⁶	SF, Class K @ Tcase = 55 °C	-	2.47	-	MHr

1. Half load at +Vout and half load at -Vout
2. Up to 60% of the total power or current can be drawn from either of the two outputs
3. Time for output voltage to settle within 1% of steady-state value
4. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified

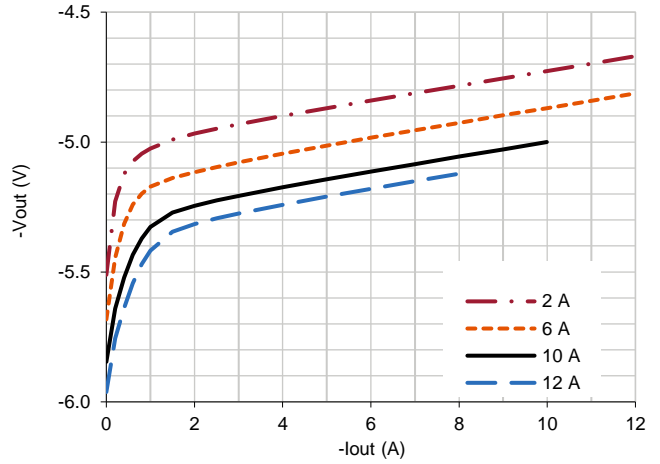
5. End-of-Life performance includes aging and radiation degradation and is within standard limits except where noted
6. Correction factor of 0.12 added to ceramic capacitors
7. 37.5 V Max continuous to be compliant to MIL-HDBK-1547 and Aerospace TOR
8. 5% load to full load at -55 °C

4.0 PERFORMANCE CURVES

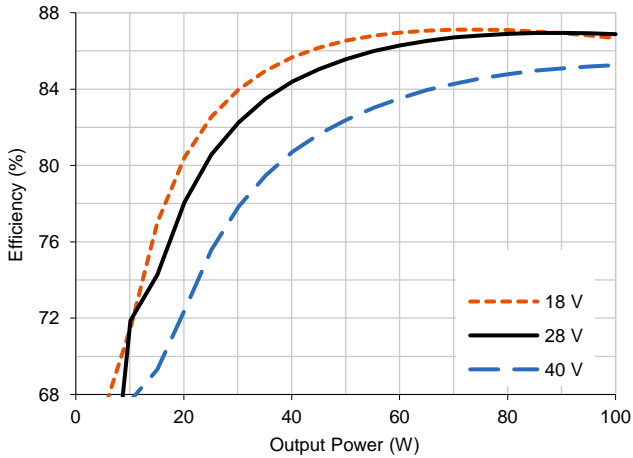
4.1.1 SVRFL2805D Efficiency (Typical, 25 °C)



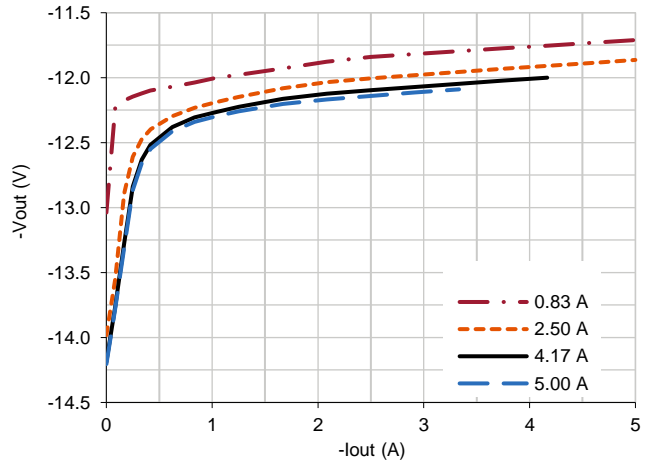
4.1.2 SVRFL2805D Cross-Regulation (Typical, 25 °C)



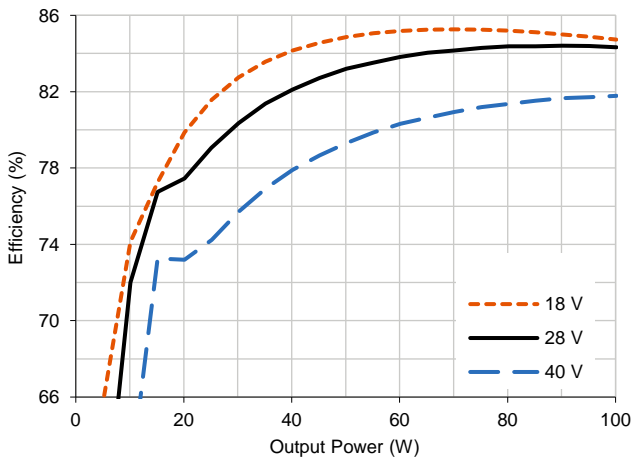
4.2.1 SVRFL2812D Efficiency (Typical, 25 °C)



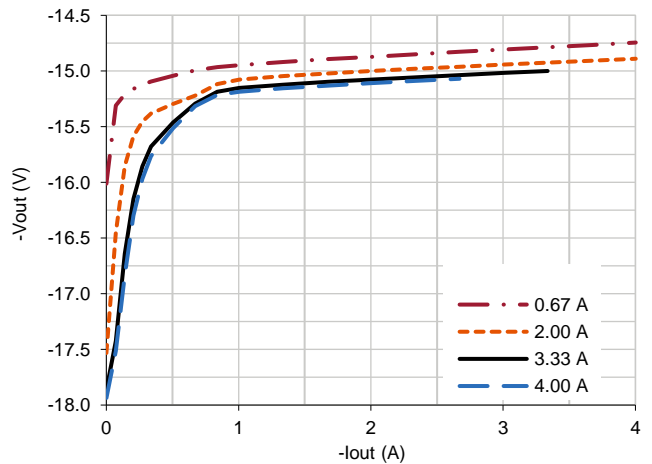
4.2.2 SVRFL2812D Cross-Regulation (Typical, 25 °C)



4.3.1 SVRFL2815D Efficiency (Typical, 25 °C)

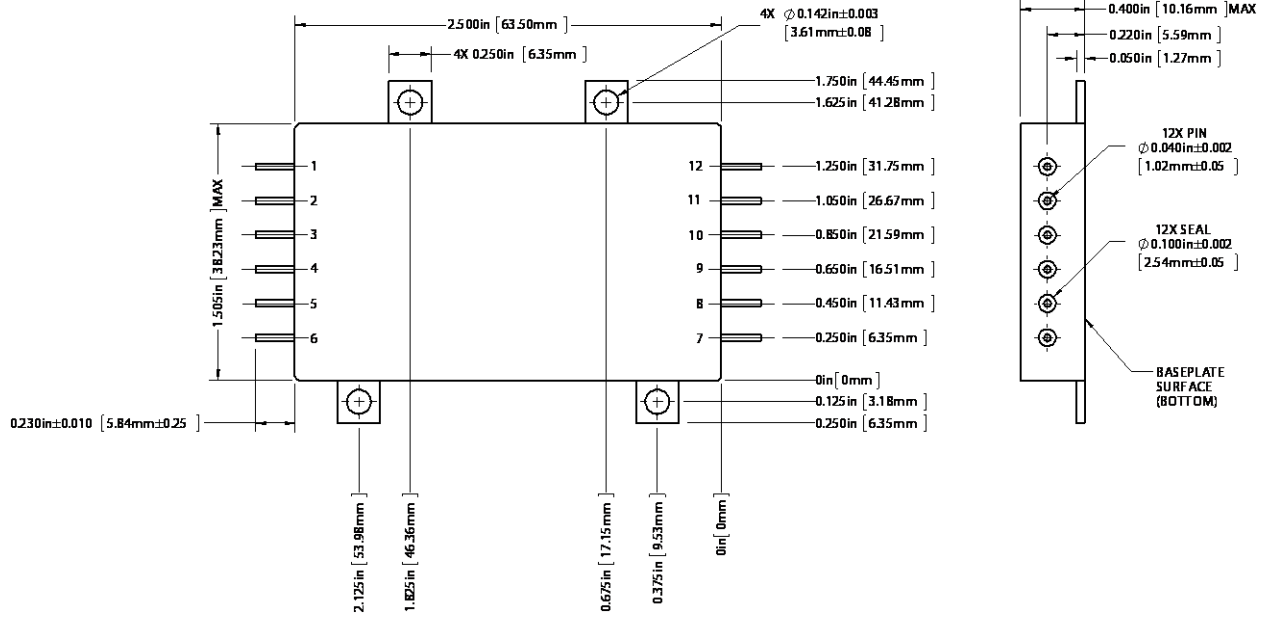


4.3.2 SVRFL2815D Cross-Regulation (Typical, 25 °C)



5.0 MECHANICAL OUTLINES AND PINOUT (CONTINUED)

Optional Side-Flanged Package:



1. Tolerances are +0.005" unless otherwise stated
2. Case temperature is measured on the center of the baseplate surface
3. Mounting holes are not threaded. Recommended fastener is 4-40
4. Materials: Case (Steel, gold over nickel plated); Cover (Kovar, nickel plated); Pin (Copper-cored alloy 52, gold over nickel plated); Pin Seals (Glass)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	28VIN	4	INH1	7	+VOUT	10	TRIM
2	INCOM	5	SYNCOUT	8	OUTCOM	11	SHARE
3	CASE	6	SYNCIN	9	-VOUT	12	INH2

6.0 TECHNICAL NOTES



Please note that many of these functions are also demonstrated in detail on the VPT website in the form of [technical video labs](#).



6.1 GENERAL INFORMATION

6.1.1 Topology Description

The SVRFL2800D Series is an isolated dual-output flyback converter. It provides a positive and negative output voltage with respect to the OUTCOM pin. Up to 60% of the total output power is available from either output. The internal voltage regulation loop actively regulates the positive output using VPT's proprietary magnetic feedback technology. The negative output is regulated by cross-regulation of the transformer windings. The negative output is well-regulated for balanced load conditions. For unbalanced load conditions, refer to the cross regulation performance graphs in Section 4.2 for expected performance. For a balanced or near-balanced load condition, the converter will regulate down to zero load, and no minimum load is required. For an unbalanced load condition, with negative loads greater than 10%, a minimum load of 10% is recommended on the positive output.

6.1.2 External Components

The SVRFL2800D Series is designed to operate stand-alone in most applications. It does not require any external components for proper operation or to meet the datasheet specifications. Input and output L-C filters are provided internally for low ripple and noise. To further reduce output ripple and noise, a small ceramic capacitor, 1 μF to 10 μF , can be added at the output. Most application specific ripple requirements can be met with the addition of output capacitors alone. External output capacitance can be added up to the maximum listed in Section 3.2.

6.1.3 Source Impedance

The impedance of the 28 V input source can interact with the DC-DC converter and can affect performance. High source impedance is often caused by a long input cable or components added in series with the input. Source resistance will cause a DC voltage drop as the converter draws DC input current. This voltage drop is simply the cable resistance multiplied by the input current at low line. The voltage drop and the actual voltage at the input to the converter will determine the minimum source voltage at which the converter will operate. A high source inductance can interact with the feedback control loop of the converter. VPT's EMI filters will usually isolate the source and eliminate this problem. In some cases, additional input capacitance will be needed to stabilize the system.

6.1.4 Output Configurations

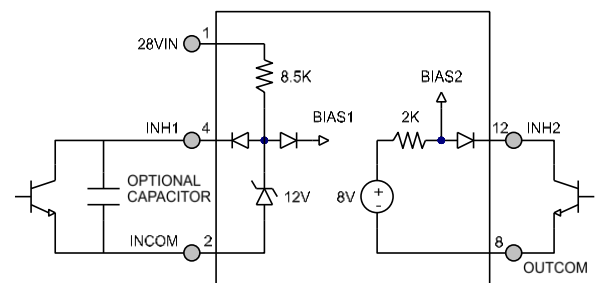
Since the converter is isolated, the outputs can be used as a traditional dual-output, with a positive and negative voltage referenced to OUTCOM, or as a single-ended output referenced to $-V_{\text{OUT}}$ or $+V_{\text{OUT}}$. For example, the SVRFL2812D model can provide +12 V and -12 V in the traditional dual output configuration, or can provide +24 V referenced to $-V_{\text{OUT}}$, or -24 V referenced to $+V_{\text{OUT}}$ in single-ended configuration. In the single-ended configuration, the OUTCOM pin will be at +12 V relative to $-V_{\text{OUT}}$.

The outputs of multiple converters can be stacked in series to provide higher voltages. When outputs of multiple modules are stacked, they naturally share the load. For example, two SVRFL2812D converters can be stacked to provide a 48 V output at 200 W.

6.2 FUNCTION DESCRIPTIONS

6.2.1 On/Off Control (INH1 and INH2)

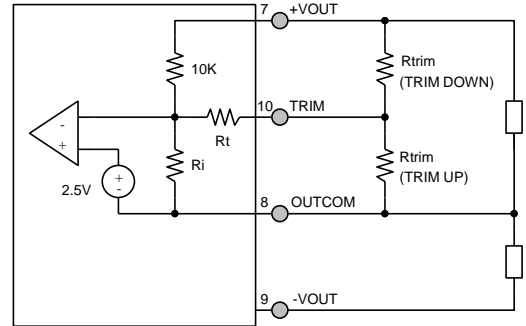
The INH1 (Inhibit 1) pin is a primary-side control pin referenced to IN COM. The INH1 pin must be driven using an open collector or open drain configuration. Pulling the INH1 pin low disables the converter output, removes bias voltage from internal control circuitry, and puts the converter in a state of minimum input current draw. Leaving INH1 open enables the output, allowing the converter to operate normally. The pin must be pulled below 1.5 V to disable the output. An optional capacitor from INH1 to INCOM may be used to delay turn-on. The INH1 pin should be left open if not used.



The INH2 (Inhibit 2) pin is a secondary-side control pin referenced to OUTCOM. The INH2 pin must also be driven in an open collector or open drain configuration. Pulling INH2 low to OUTCOM disables the converter output. Internal control circuits, however, remain active. The pin must be pulled below 1.0 V to disable the output. The INH2 pin should be left open if not used.

6.2.2 Adjusting the Output Voltage (TRIM)

The output voltage set point of the converter can be adjusted using the TRIM pin. To adjust the output up, connect the trim resistor from TRIM to OUTCOM. To adjust the output down, connect the trim resistor from TRIM to +VOUT. The maximum trim range is -20% and +10% from nominal. The appropriate resistor values versus the output voltage are given in the table below. Because the TRIM pin can be sensitive to external noise, the trim resistor should be physically located close to the SVRFL converter with short interconnects. The TRIM pin should be left open if not used. When adjusting the output voltage, do not exceed the rated total output power or output current.



SVRFL2805D		SVRFL2812D		SVRFL2815D	
+Vout (V)	Rtrim (Ω)	+ Vout (V)	Rtrim (Ω)	+ Vout (V)	Rtrim (Ω)
5.5	35k	13.2	5.8k	16.50	1.7k
5.4	47.5k	13.0	10k	16.25	5k
5.3	68.3k	12.8	16.2k	16.00	10k
5.2	110k	12.6	26.6k	15.75	18.3k
5.1	235k	12.4	47.3k	15.50	35k
5.0		12.2	109k	15.25	85k
4.9	225k	12.0		15.00	
4.8	100k	11.8	454k	14.75	475k
4.7	58.3k	11.6	213k	14.50	225k
4.6	37.5k	11.4	134k	14.25	142k
4.5	25k	11.2	94k	14.00	100k
4.4	16.7k	11.0	70.1k	13.75	75k
4.3	10.7k	10.8	54.3k	13.50	58.3k
4.2	6.3k	10.6	42.9k	13.25	46.4k
4.1	2.8k	10.4	34.4k	13.00	37.5k
4.0	0	10.2	27.8k	12.75	30.6k
		10.0	22.5k	12.50	25k
		9.8	18.2k	12.25	20.5k
		9.6	14.6k	12.00	16.7k

6.2.3 Frequency Synchronization (SYNCIN, SYNCOUT)

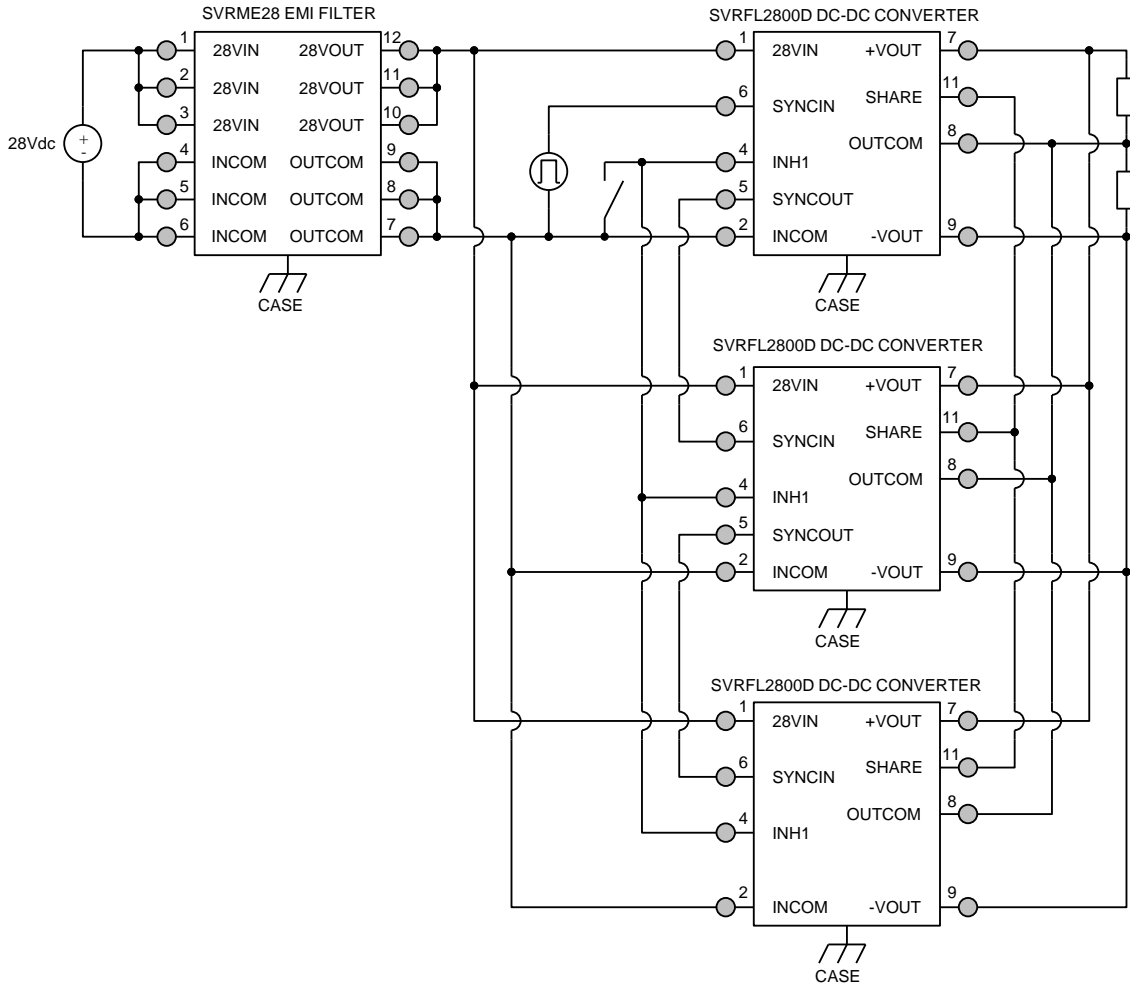
The SVRFL2800D Series will free run at a switching frequency of approximately 550 kHz, which has been set for optimum converter performance. Frequency synchronization is not necessary unless required by system constraints. The SVRFL2800D Series provides a frequency synchronization input (SYNCIN) and output (SYNCOUT), both referenced to INCOM.

The SYNCIN pin can be driven by an external clock or by the SYNCOUT pin of another SVRFL converter. The internal clock and internal power train will operate at the frequency applied to the SYNCIN pin. The SYNC IN pin should be driven with a TTL type 5 V square wave signal. The duty cycle of the square wave should be between 20% and 80%. The SYNCIN pin is internally capacitively-coupled and the internal load is equivalent to 220 pF. Proper layout and circuit techniques are necessary to prevent noise from being injected into this pin. Synchronized converters should be located physically close together and share a low impedance INCOM connection. The SYNCIN pin can be left open or connected to INCOM if not used.

The SYNCOUT pin provides a 5 V quasi-square wave output at either the SYNCIN frequency or the free-running frequency if SYNCIN is not used. The SYNCOUT of a SVRFL can be connected to the SYNCIN pin of a second SVRFL to synchronize its switching frequency to that of the first SVRFL. Similarly, the SYNCOUT of the second SVRFL can be connected to SYNCIN of a third SVRFL. Subsequent SVRFL converters can be connected in this daisy chain arrangement as shown in the figure. SYNCOUT should be left open if not used.

6.2.4 Parallel Operation (SHARE)

The SVRFL2800D Series provides a SHARE function for active current sharing among paralleled modules. For the dual output model, the SHARE function is only applicable in the single-ended output configuration (see section 6.1.4) where no current is drawn from the OUTCOM pin. To enable load sharing, connect a single wire between the SHARE pins of all parallel modules. The SHARE pin can be noise sensitive. Paralleled converters should be located physically close to one another and share a low impedance OUTCOM connection. A symmetrical layout of the output traces will improve share accuracy. Frequency synchronization is not required for parallel operation. The SHARE pin should be left open if not used.



6.3 PROTECTION FEATURES

6.3.1 Input Undervoltage Lockout

The SVRFL2800D Series provides input undervoltage lockout protection. For input voltages below the turn-on voltage, the converter will remain off, drawing minimal current from the source. When the input voltage exceeds the turn-on voltage, the converter will start. The lockout circuit is designed to tolerate slow ramping input voltage waveforms. VPT's proprietary magnetic feedback technology provides bias voltage to all secondary control circuits and control amplifiers before the output starts, ensuring a well-controlled start up sequence.

6.3.2 Output Soft Start

The SVRFL2800D Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage-mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately 4 ms. The soft-start function is active whether the module is turned on with an application of input voltage or from release of the inhibit pin. Under normal conditions, current drawn from the source during turn on will not exceed the full load input current. The turn-on delay time is specified from the application of input voltage (or release of the inhibit pin) until the output reaches 90% of its final value.

6.3.3 Output Overcurrent Protection

The SVRFL2800D Series provides output overcurrent and output short circuit protection. During a load fault condition, a constant output current control circuit reduces the converter duty cycle to limit the total output current to approximately 125% its rated value. The current limit protection circuit limits the sum of output currents in both +Vout and -Vout. It does not distinguish if the current is on the positive or negative output. The converter will continue to provide constant current into any overload or short circuit condition. This feature allows the converter to start into any capacitive load. Recovery is automatic and immediate upon removal of the fault condition. Sustained short circuit or overload operation can cause excessive power dissipation. Care should be taken to control the operating temperature of the converter in this condition.

6.4 THERMAL CONSIDERATIONS

The SVRFL2800D Series is rated for full power operation at 125 °C. Operation above 125 °C is allowed at reduced power. Specifically, the output power should be derated linearly from full power at 125 °C to half power at 130 °C and to zero power at 135 °C. The operating temperature of the converter is specified on the baseplate of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB or other thermal surface. The internal power dissipating components are mounted to the baseplate of the converter and all heat flow is through the baseplate and mounting flanges. The lid of the converter does not provide a good thermal path.

The hybrid DC-DC converter contains many semiconductor components. The maximum temperature rise from junction to case is 20 °C at full load.

6.5 RADIATION HARDNESS ASSURANCE

VPT takes a conservative approach to radiation testing to ensure product performance in a space environment. VPT's DLA-approved Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for guaranteeing the performance of VPT products under various environmental conditions in space including Total Ionizing Dose (TID) and Single-Event Effects (SEE). Additionally, Enhanced Low Dose-Rate Sensitivity (ELDRS) effects are considered for all bipolar ICs used in the hybrid. Hardness is guaranteed by a combination of both hybrid-level characterization and Radiation Lot Acceptance Testing (RLAT) of all sensitive semiconductor piece-parts used within the hybrid.

6.5.1 Radiation Test and Performance Levels

Radiation Environment		Piece Part RLAT	Hybrid-Level Characterization
Total Ionizing Dose (TID)	High Dose Rate (HDR)	100 krad(Si)	100 krad(Si)
	Low Dose Rate (LDR)	¹ 100 krad(Si)	100 krad(Si)
Single-Event Effects (SEE)	Destructive (SEB, SEGR, SEL)	Not applicable	≥ 85 MeV/mg/cm ²
	² Non-Destructive (SET, SEU, SEFI)	Not applicable	≥ 85 MeV/mg/cm ²

1. Piece-part LDR screening performed only on potentially ELDRS parts (bipolar ICs).
2. The PWM IC used in this part is susceptible to a non-destructive SEFI/SEL event with threshold LET ≥ 42 MeV/mg/cm². The SEFI manifests as a shutdown for up to 1 second followed by a controlled soft-start of the converter. The non-destructive SEL manifests itself as a shutdown requiring user intervention to recover by cycling either the input power or the inhibit function. At the worst-case 125 °C and 85 MeV/mg/cm², the cross-section of these events is 3.18 x 10⁻⁶ cm². Full details available in the Radiation Test Report.

6.5.2 RHA Plan Summary

Test	RHA Plan for SVR Series Isolated DC-DC Converters
Total Ionizing Dose (TID):	Sensitive semiconductor components undergo RLAT to 100 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 100 krad(Si).
Enhanced Low Dose Rate Sensitivity (ELDRS):	All bipolar linear ICs are characterized for ELDRS and tested in accordance with MIL-STD-883 test method 1019 section 3.13
Single Event Effects (SEE):	Converters are characterized to LET ≥ 85 MeV/mg/cm ² for both catastrophic events (SEL, SEB, SEGR) and functional interrupts (SEFI) under heavy ion exposure. Converters are also characterized for cross-section and magnitude of output transients (SET) for at least 3 different LET levels.
Radiation Lot Acceptance Testing (RLAT):	All production lots of sensitive semiconductor components undergo RLAT for TID at HDR and/or LDR as appropriate per part type.

6.5.3 RHA Designators available on SMD

The SVRFL2800D series converters are available on SMD with RHA level R. See section 8.0 for full SMD number information.

6.5.4 Supporting Documentation Available (Contact Sales)

- Radiation Hardness Assurance Plan: DLA-approved RHA plan covering TID, SEE, and ELDRS
- Worst-Case Analysis Report: Detailed worst-case analysis including electrical stress/derating limits and guaranteed circuit performance post-radiation and end of life
- Radiation Test Summary Report: Overview of piece-part RLAT and hybrid characterization for all guaranteed environments. Also includes SEE cross-section data.
- Reliability Report: MTBF report based on MIL-HDBK-217 reliability calculations.
- Thermal Analysis Report: Component temperature rise analysis and measurement results.

7.0 ENVIRONMENTAL SCREENING

100% tested per MIL-STD-883 as referenced to MIL-PRF-38534.

Contact sales for more information concerning additional environmental screening and testing options. VPT Inc. reserves the right to ship higher screened or SMD products to meet orders for lower screening levels at our sole discretion unless specifically forbidden by customer contract.

Test	MIL-STD-883 Test Method, Condition	/H+ (Class H + PIND)	/K (Class K)	/EM (Engineering Model) Non-QML ^{1,6}
Non-Destructive Bond Pull	TM2023	• ²	•	• ²
Internal Visual	TM2010, TM2017, TM2032 (MIL-STD-750, TM2072, TM2073)	•	•	•
Temperature Cycling	TM1010, Condition C -65 °C to 150 °C, Ambient	•	•	
Constant Acceleration	TM2001, 3000g, Y1 Direction	•	•	
PIND ³	TM2020, Condition A	• ²	•	
Pre Burn-In Electrical	25 °C		•	
Burn-In	TM1015, 320 hrs., 125 °C, Case Typ		•	
	TM1015, 160 hrs., 125 °C, Case Typ	•		
	24 hrs., 125 °C, Case Typ			•
Final Electrical	MIL-PRF-38534, Group A Subgroups 1-6 -55 °C, 25 °C, 125 °C ⁴	•	•	
	MIL-PRF-38534, Group A Subgroups 1 and 4 25 °C			•
Hermeticity (Seal)	TM1014, Fine Leak, Condition A2 or B1	•	•	
	TM1014, Gross Leak, Condition C1 or B2	•	•	
	Gross Leak, Dip (1x10 ⁻³)			•
Radiography ⁵	TM2012		•	
External Visual	TM2009	•	•	•

1. Non-QML products may not meet all requirements of MIL-PRF-38534
2. Not required per MIL-PRF-38534. Test performed for additional product quality assurance
3. PIND test Certificate of Compliance included in product shipment

4. 100% R&R testing with all test data included in product shipment
5. Radiographic test Certificate of Compliance and film(s) or data CD included in product shipment
6. Engineering models utilize only the screening specified and are not considered compliant for flight use

8.0 STANDARD MICROCIRCUIT DRAWING (SMD) NUMBERS

Standard Microcircuit Drawing Number	SVRFL2800D Series Similar Part Number
5962R1323401HXC	SVRFL2805D/H+
5962R1323401HXA	SVRFL2805D/H+-E
5962R1323401KXC	SVRFL2805D/K
5962R1323401KXA	SVRFL2805D/K-E
5962R1323401HYC	SVRFL2805DF/H+
5962R1323401HYA	SVRFL2805DF/H+-E
5962R1323401KYC	SVRFL2805DF/K
5962R1323401KYA	SVRFL2805DF/K-E
5962R1323402HXC	SVRFL2812D/H+
5962R1323402HXA	SVRFL2812D/H+-E
5962R1323402KXC	SVRFL2812D/K
5962R1323402KXA	SVRFL2812D/K-E
5962R1323402HYC	SVRFL2812DF/H+
5962R1323402HYA	SVRFL2812DF/H+-E
5962R1323402KYC	SVRFL2812DF/K
5962R1323402KYA	SVRFL2812DF/K-E
5962R1323403HXC	SVRFL2815D/H+
5962R1323403HXA	SVRFL2815D/H+-E
5962R1323403KXC	SVRFL2815D/K
5962R1323403KXA	SVRFL2815D/K-E
5962R1323403HYC	SVRFL2815DF/H+
5962R1323403HYA	SVRFL2815DF/H+-E
5962R1323403KYC	SVRFL2815DF/K
5962R1323403KYA	SVRFL2815DF/K-E

Do not use the SVRFL2800D Series similar part number for SMD product acquisition. It is listed for reference only. For exact specifications for the SMD product, refer to the SMD drawing. SMDs can be downloaded from the DLA Land and Maritime (Previously known as DSCC) website at <https://landandmaritimeapps.dla.mil/programs/defaultapps.asp>. The SMD number listed above represents the Federal Stock Class, Device Type, Device Class Designator, Case Outline, Lead Finish and RHA Designator (where applicable). Please reference the SMD for other screening levels, lead finishes, and radiation levels. All SMD products are marked with a "Q" on the cover as specified by the QML certification mark requirement of MIL-PRF-38534.

9.0 ORDERING INFORMATION

SVRFL	28	05	D	F	/K	-	XXX
1	2	3	4	5	6		7

(1) Product Series	(2) Nominal Input Voltage	(3) Output Voltage	(4) Number of Outputs	(5) Package Option	(6) Screening Code ^{1,2,3}	(7) Additional Screening Code
SVRFL	28 28 Volts	05 5 Volts 12 12 Volts 15 15 Volts	D Dual	(None) Standard F Side-Flanged	/EM Engineering Model /H+ Class H + PIND /K Class K	Contact Sales

- 1 Contact the VPT Sales Department for availability of Class H (/H) or Class K (/K) qualified products
- 2 VPT Inc. reserves the right to ship higher screened or SMD products to meet lower screened orders at our sole discretion unless specifically forbidden by customer contract
- 3 Engineering models utilize only the standard screening specified and are not considered compliant for flight use. These models are intended for low volume engineering characterization only and have no guarantee regarding operation in a radiation environment. The customer must place the following statement on each line item of their purchase order(s) for /EM units when ordering engineering models:

"(Customer Name) acknowledges that the /EM unit listed in this line item is not permitted for flight use and will be used for Engineering characterization only."

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, source inspection, and/or special element evaluation for space or other higher quality applications.

10.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

Phone: (425) 353-3010
Fax: (425) 353-4030
E-mail: vptsales@vptpower.com

All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

11.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

[Product Catalogs](#)



[Application Notes and White Papers](#)



[Technical Video Labs](#)



[Additional Products For Avionics/Military, Hi-Rel COTS, and Space Applications](#)

